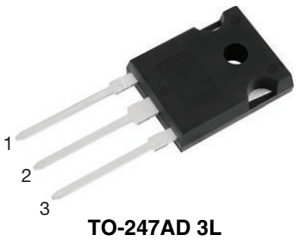
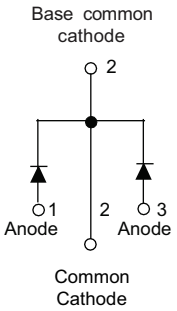
650 V Gen 4 Power Silicon Carbide Schottky Diode, 2 x 20 A



TO-247AD 3L



FEATURES

- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- AEC-Q101 qualified meets JESD 201 class 2 whisker test
- Solder bath temperature 275 °C maximum, 10 s per JESD 22-B106
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

LINKS TO ADDITIONAL RESOURCES

3D Models

PRIMARY CHARACTERISTICS	
I_F	2 x 20 A
V_R	650 V
V_F at I_F at 25 °C, typ.	1.33 V
T_J max.	175 °C
I_R at V_R at 175 °C	110 µA
Q_C (V_R = 400 V)	52 nC
Package	TO-247AD 3L
Circuit configuration	Common cathode

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimized for extreme high speed hard switching across a wide temperature range. This SiC diode is ideal for applications with high dI/d_t such as high efficiency PFC and ultra-high frequency output rectifiers in AC/DC and DC/DC converters.

MECHANICAL DATA

Case: TO-247AD 3L

Molding compound meets UL 94 V-0 flammability rating Base P/NHM3 - halogen-free, RoHS-compliant, and AEC-Q101 qualified

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Mounting torque: 10 in-lbs maximum

MAXIMUM RATINGS (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage per leg	V_{RRM}		650	V
Continuous forward current per leg	I_F (1)	T_C = 150 °C (DC)	20	A
	I_F (2)	T_C = 137 °C (DC)	20	A
DC blocking voltage per leg	V_{DC}		650	V
Repetitive peak forward current per leg	I_{FRM}	T_C = 25 °C, f = 50 Hz, square wave, DC = 25 %	82	A
Non-repetitive peak forward surge current per leg	I_{FSM}	T_C = 25 °C, t_p = 10 ms, half sine wave	125	A
		T_C = 110 °C, t_p = 10 ms, half sine wave	115	
Power dissipation per leg	P_{tot} (1)	T_C = 25 °C	188	W
		T_C = 110 °C	81	
	P_{tot} (2)	T_C = 25 °C	125	W
		T_C = 110 °C	54	
I^2t value per leg	$\int i^2 dt$	T_C = 25 °C	78	A^2s
		T_C = 110 °C	66	
Operating junction and storage temperatures	T_J (3), T_{Stg}		-55 to +175	°C

Notes

(1) Based on typical R_{th}

(2) Based on maximum R_{th}

(3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage per leg	V_F	I_F = 20 A	-	1.33	1.5	V
		I_F = 20 A, T_J = 150 °C	-	1.5	1.75	
		I_F = 20 A, T_J = 175 °C	-	1.6	-	
Reverse leakage current per leg	I_R	V_R = V_R rated	-	4.5	145	µA
		V_R = V_R rated, T_J = 150 °C	-	55	300	
		V_R = V_R rated, T_J = 175 °C	-	110	-	
Total capacitance per leg	C	V_R = 1 V, f = 1 MHz	-	860	-	pF
		V_R = 400 V, f = 1 MHz	-	74	-	
Total capacitive charge per leg	Q_C	V_R = 400 V, f = 1 MHz	-	52	-	nC

THERMAL - MECHANICAL SPECIFICATIONS (T_A = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction-to-case	per leg	R_{thJC}	-	0.8	1.2	°C/W
	per device		-	0.4	0.6	°C/W
Marking device			4C40CP07L			

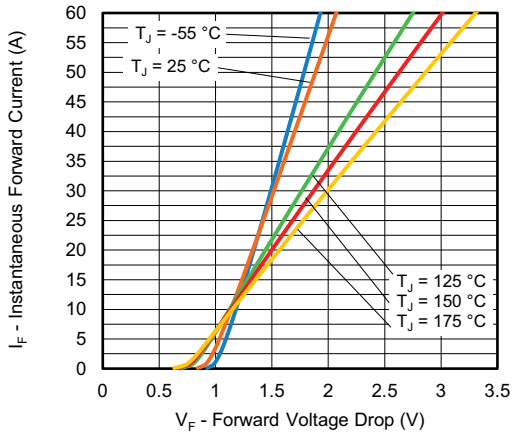


Fig. 1 - Typical Forward Voltage Drop Characteristics Per Leg

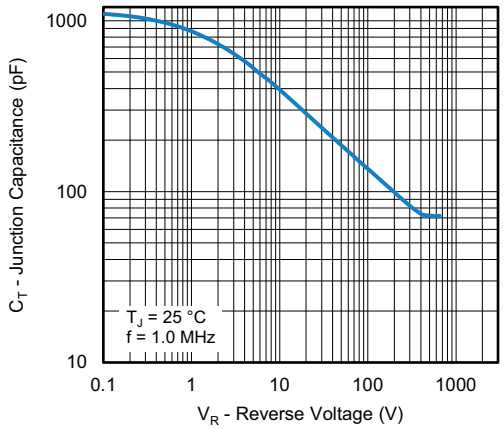


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage Per Leg

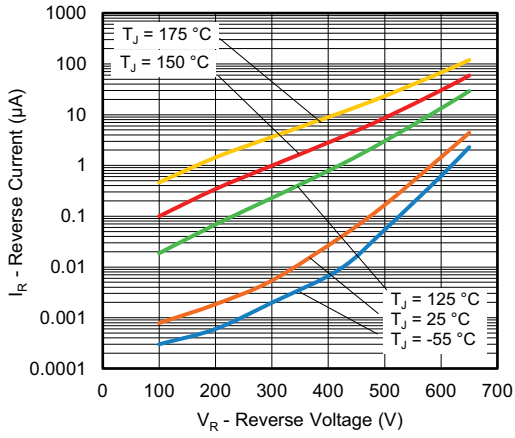


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage Per Leg

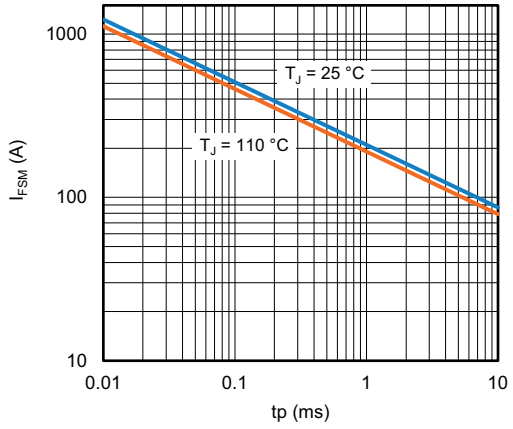


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave) Per Leg

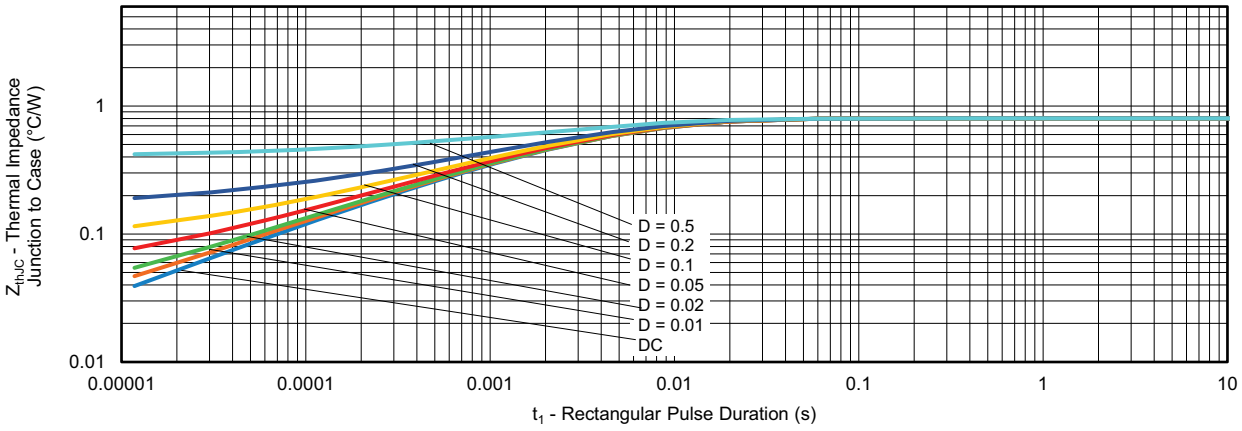


Fig. 5 - Typical Thermal Impedance Z_{thJC} - Characteristics Per Leg

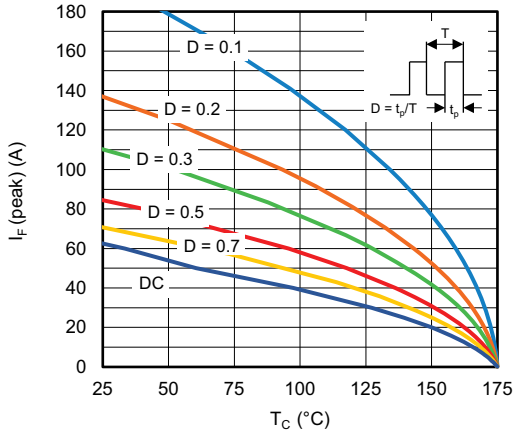


Fig. 6 - Peak Forward Current vs.
Maximum Allowable Case Temperature Per Leg

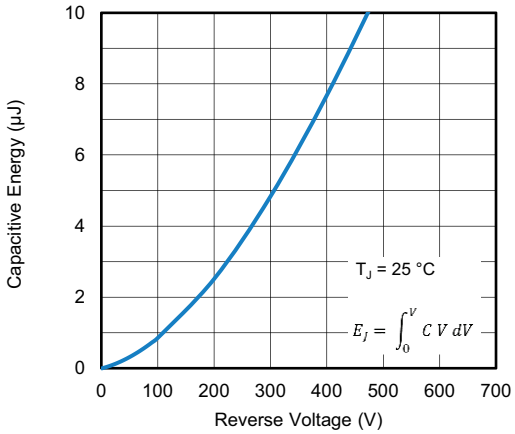


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage Per Leg

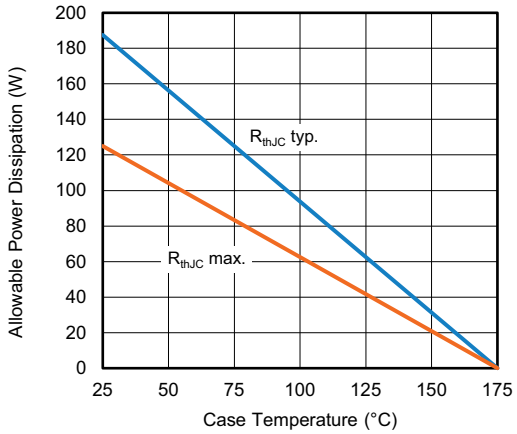


Fig. 7 - Forward Power Loss Characteristics Per Leg

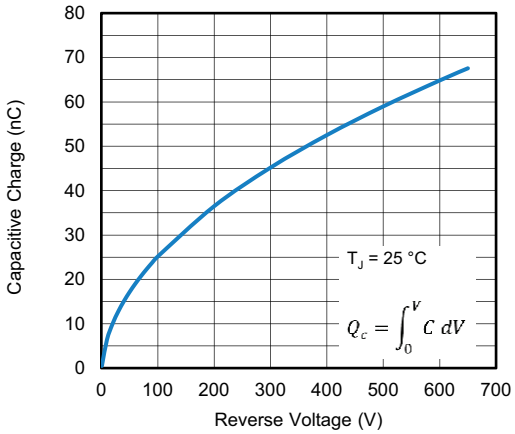
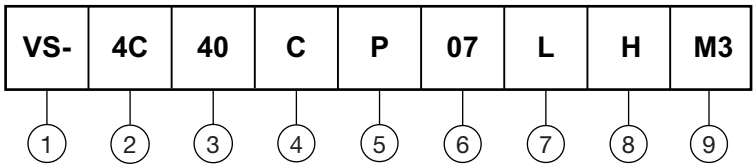


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage Per Leg

ORDERING INFORMATION TABLE

Device code



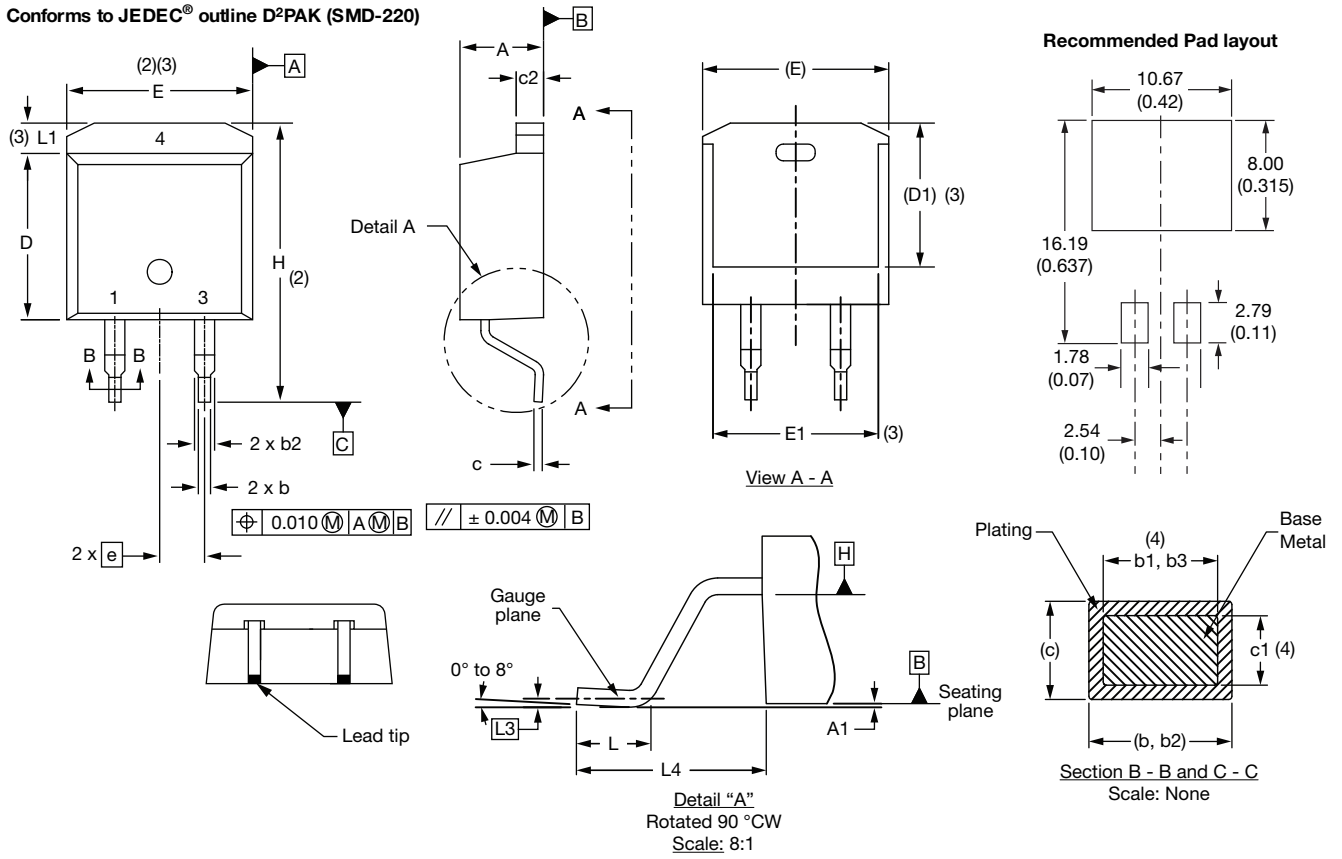
1 - Vishay Semiconductors product
2 - 4C = SiC diode, Generation 4
3 - Current rating (40 = 40 A)
4 - C = common cathode
5 - P = package TO-247
6 - Voltage rating: 07 = 650 V
7 - L = long lead
8 - H = AEC-Q101 qualified
9 - Environmental digit:
M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

ORDERING INFORMATION			
PREFERRED P/N	**UNIT WEIGHT**	**BASE QUANTITY**	**PACKAGING DESCRIPTION**
VS-4C40CP07LHM3	5.5 g	25 / tube	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95626
Part marking information	www.vishay.com/doc?95007
SPICE model	www.vishay.com/doc?97487

D²PAK 2L (TO-263AB 2L)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

Notes

(1) Dimensioning and tolerancing per ASME Y14.5 M-1994

(2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body

(3) Thermal pad contour optional within dimension E, L1, D1 and E1

(4) Dimension b1 and c1 apply to base metal only

(5) Datum A and B to be determined at datum plane H

(6) Controlling dimension: inch

(7) Outline conforms to JEDEC® outline TO-263AB

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