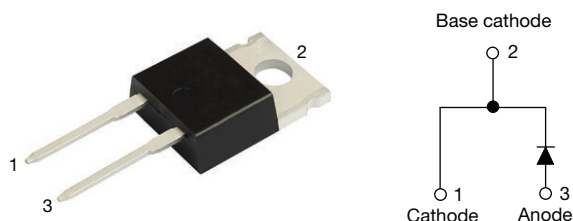


650 V Gen 4 Power Silicon Carbide Schottky Diode, 16 A



FEATURES

- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- AEC-Q101 qualified meets JESD 201 class 2 whisker test
- Solder bath temperature 275 °C maximum, 10 s per JESD 22-B106
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

LINKS TO ADDITIONAL RESOURCES



3D Models

PRIMARY CHARACTERISTICS

$I_{F(AV)}$	16 A
V_R	650 V
V_F at I_F at 25 °C, typ.	1.3 V
T_J max.	175 °C
I_R at V_R at 175 °C	94 μ A
Q_C ($V_R = 400$ V)	44 nC
Package	TO-220AC 2L
Circuit configuration	Single

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimized for extreme high-speed hard switching across a wide temperature range. This SiC diode is ideal for applications with high dI/dt such as high efficiency PFC and ultra-high frequency output rectifiers in AC/DC and DC/DC converters

MECHANICAL DATA

Case: TO-220AC 2L

Molding compound meets UL 94 V-0 flammability rating
Base P/NHM3 - halogen-free, RoHS-compliant, and AEC-Q101 qualified

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Mounting torque: 10 in-lbs maximum

MAXIMUM RATINGS ($T_A = 25$ °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Continuous forward current	$I_F^{(1)}$	$T_C = 139$ °C (DC)	16	A
	$I_F^{(2)}$	$T_C = 135$ °C (DC)	16	A
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	$T_C = 25$ °C, $f = 50$ Hz, square wave, DC = 25 %	66	A
Non-repetitive peak forward surge current	I_{FSM}	$T_C = 25$ °C, $t_p = 10$ ms, half sine wave	101	A
		$T_C = 110$ °C, $t_p = 10$ ms, half sine wave	90	A
Power dissipation	$P_{tot}^{(1)}$	$T_C = 25$ °C	103	W
		$T_C = 110$ °C	45	W
	$P_{tot}^{(2)}$	$T_C = 25$ °C	94	W
		$T_C = 110$ °C	41	W
I^2t value	$\int i^2 dt$	$T_C = 25$ °C	51	A ² s
		$T_C = 110$ °C	40.5	A ² s
Operating junction and storage temperatures	$T_J^{(2)}, T_{Stg}$		-55 to +175	°C

Notes

(1) Based on typical R_{th}

(2) Based on maximum R_{th}

(3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$

**ELECTRICAL SPECIFICATIONS** ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage	V_F	$I_F = 16\text{ A}$	-	1.3	1.5	V
		$I_F = 16\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$	-	1.45	1.75	
		$I_F = 16\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	-	1.55	-	
Reverse leakage current	I_R	$V_R = V_R\text{ rated}$	-	2.6	80	μA
		$V_R = V_R\text{ rated}, T_J = 150\text{ }^{\circ}\text{C}$	-	43	190	
		$V_R = V_R\text{ rated}, T_J = 175\text{ }^{\circ}\text{C}$	-	94	-	
Total capacitance	C	$V_R = 1\text{ V}, f = 1\text{ MHz}$	-	737	-	pF
		$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	63	-	
Total capacitive charge	Q_C	$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	44	-	nC

THERMAL AND MECHANICAL SPECIFICATIONS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction to case	R_{thJC}		-	1.45	1.6	$^{\circ}\text{C/W}$
Marking device				4C16ET07T		

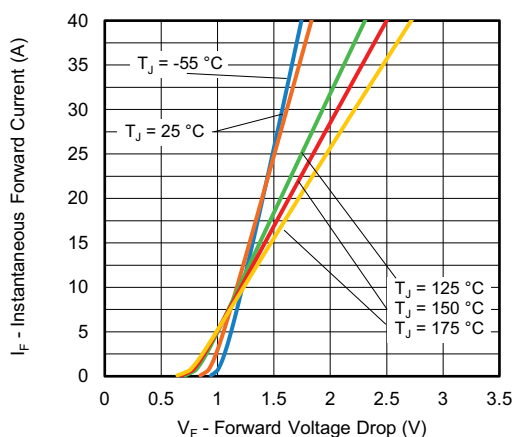


Fig. 1 - Typical Forward Voltage Drop Characteristics

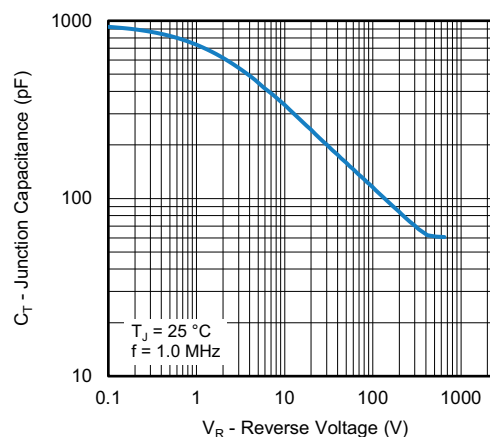


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

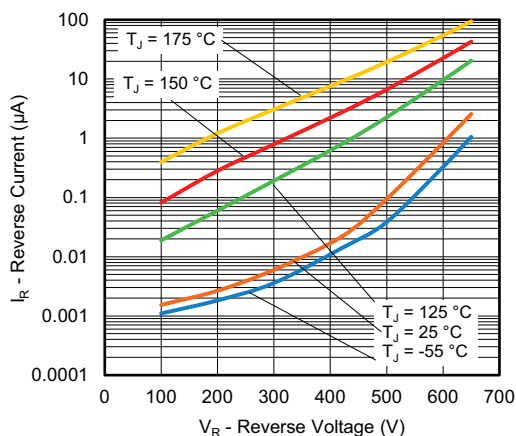


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

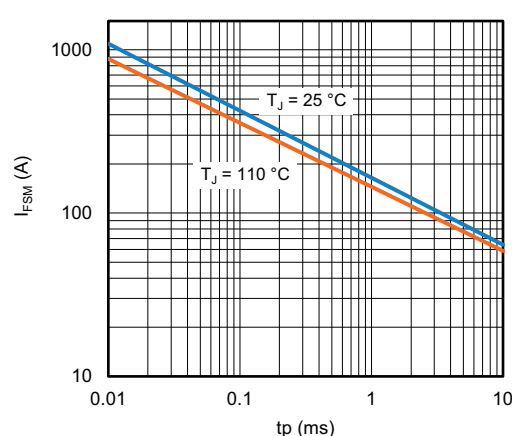


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

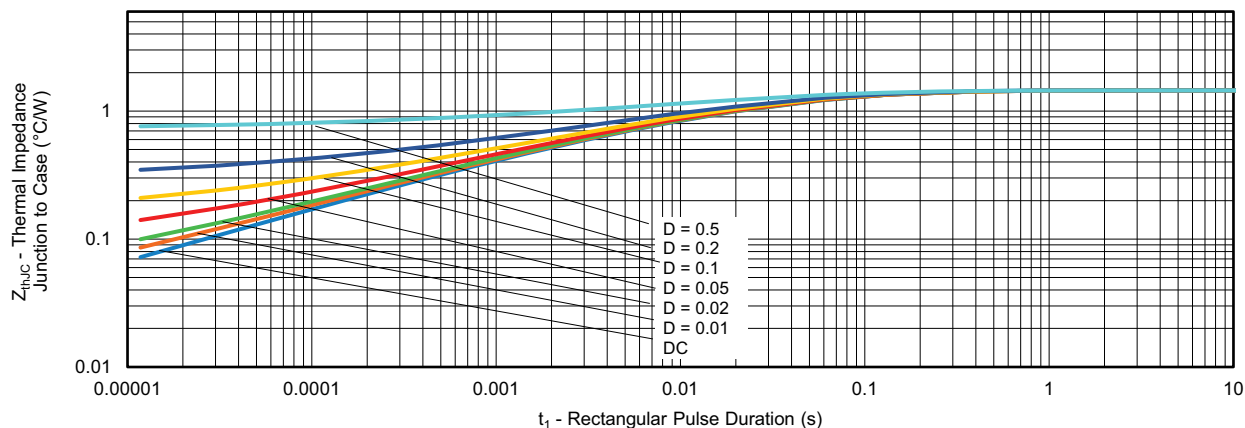
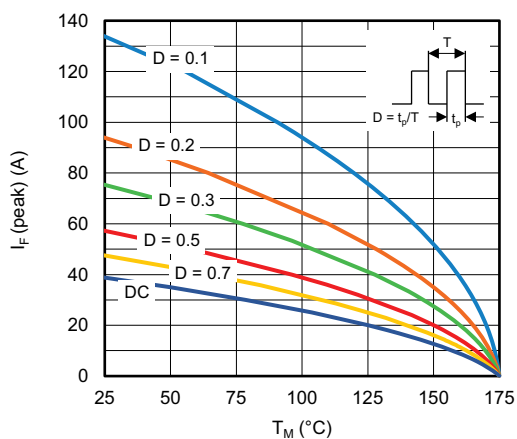

Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics


Fig. 6 - Peak Forward Current vs. Maximum Allowable Case Temperature

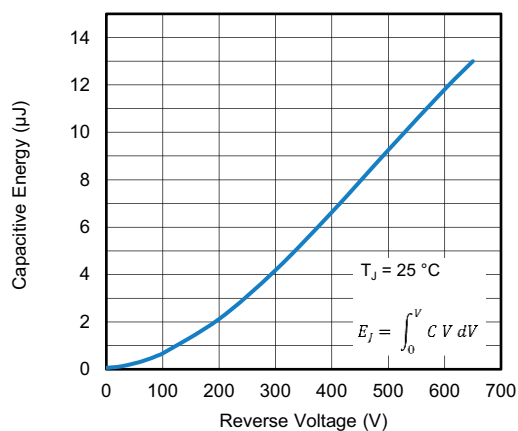


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

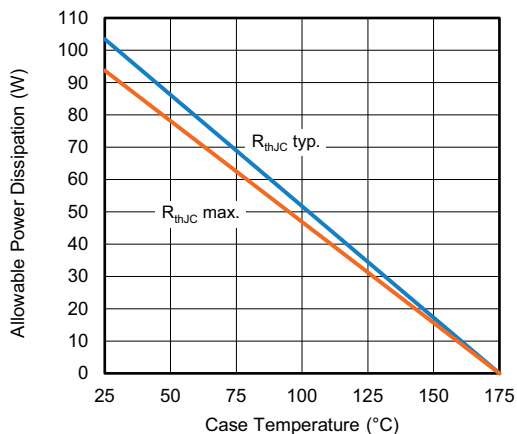


Fig. 7 - Forward Power Loss Characteristics

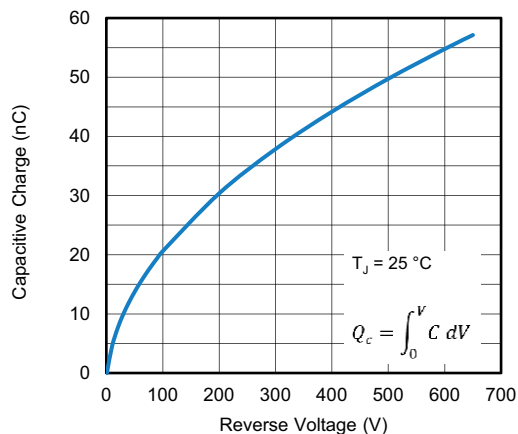


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage



ORDERING INFORMATION TABLE

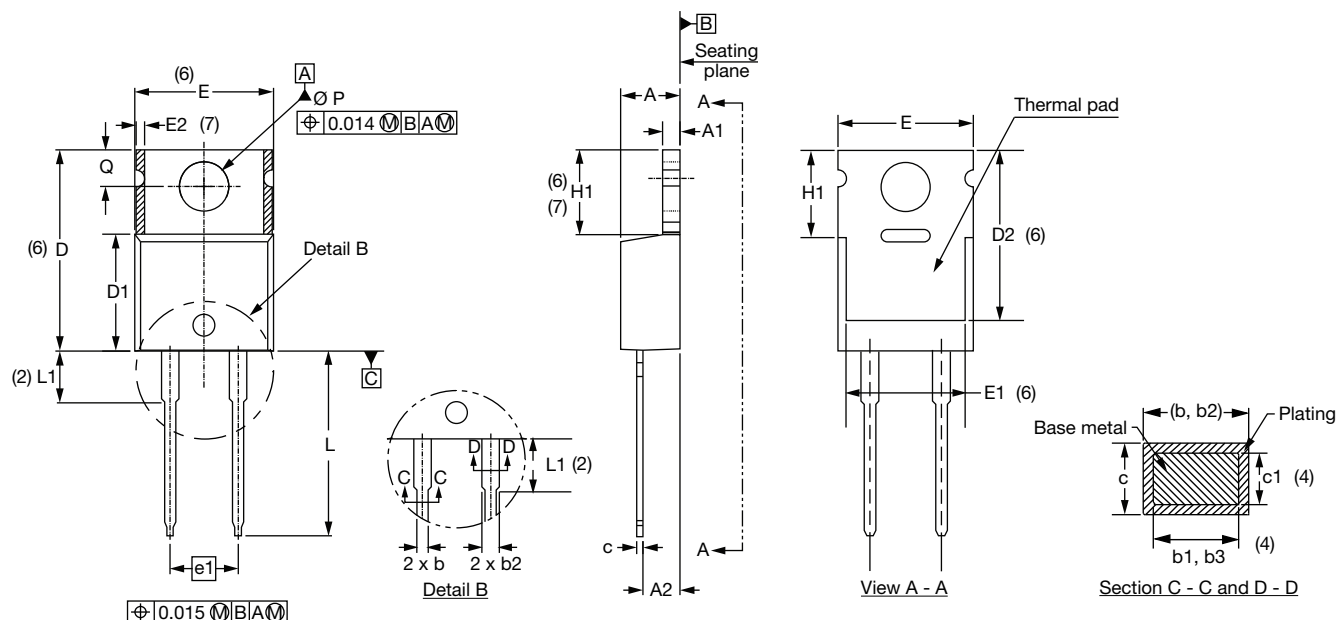
Device code	VS-	4C	16	E	T	07	T	H	M3
	1	2	3	4	5	6	7	8	9
1	- Vishay Semiconductors product								
2	- 4C = SiC diode, generation 4								
3	- Current rating (16 = 16 A)								
4	- E = single diode								
5	- T = TO-220 package								
6	- Voltage rating: (07 = 650 V)								
7	- T = true 2 pin								
8	- H = AEC-Q101 qualified								
9	- Environmental digit: M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free								

ORDERING INFORMATION			
PREFERRED P/N	UNIT WEIGHT	BASE QUANTITY	PACKAGING DESCRIPTION
VS-4C16ET07THM3	2 g	50 per tube	Antistatic plastic tube

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?96069
Part marking information	www.vishay.com/doc?95391

TO-220AC 2L

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e1	4.88	5.28	0.192	0.208	
H1	5.84	6.86	0.230	0.270	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC® TO-220, except D2, where JEDEC® minimum is 0.480"



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