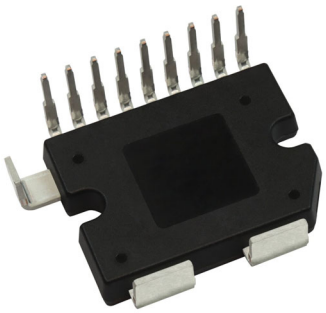
FlatPAK HC0 Transfer Mold Power Module
Half Bridge - Power MOSFET, 200 A



FEATURES

- Half bridge inverter
- Current sensing and temperature sensing
- Electrically isolated exposed DBC substrate
- C snubber for low EMI
- Qualified according to AQG324 guidelines
- PPAP capable
- Epoxy compound UL 94 V-0 certified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

PRIMARY CHARACTERISTICS	
V_{DSS}	80 V
$R_{DS(on)}$, Q1 (chip level)	0.45 mΩ
I_D	195 A at 80 °C
Type	Modules - MOSFET
Package	FlatPAK HC0

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
MOSFET				
Drain to source voltage	V_{DSS}		80	V
Continuous drain current, $V_{GS\ at}$ 10 V	I_D	T_C = 25 °C	243	A
		T_C = 80 °C	195	
		T_C = 118 °C	150	
Pulsed drain current	I_{DM}	T_C = 25 °C, t_p = 250 µs, square waveform	1050	
Pulsed source current (body diode)	I_{SM}	T_C = 150 °C, t_p = 1 ms, square waveform	1530	
Power dissipation	P_D	T_C = 25 °C	194	W
Gate to source voltage	V_{GS}		± 20	V
Single pulse avalanche energy	E_{AS}	T_C = 25 °C, L = 1 mH, V_{GS} = 10 V	1800	mJ
Single pulse avalanche current	I_{AS}	T_C = 25 °C, L = 1 mH, V_{GS} = 10 V	60	A
MODULE				
Insulation voltage (RMS)	V_{ISOL}	Any terminal to case, t = 1 s	2000	V

THERMAL- MECHANICAL SPECIFICATIONS

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction temperature range		T_J		-55	-	175	°C
Storage temperature range		T_{Stg}		-40	-	150	°C
Operating temperature range		T_{op}		-40	-	150	°C
Junction to case	MOSFET	R_{thJC}		-	-	0.77	°C/W
Case to heat sink	Module	R_{thCS}	Flat, greased surface (1)	-	0.15	-	
Package parasitic stray inductance		L_p		-	10	-	nH
Compression force			Maximum load, test speed: 0.5 mm/min (2)	3	-	22	kN
Weight				-	10	-	g
Mounting torque			Mounting screw - M3	-	0.7	-	Nm
Case style				FlatPAK HC0			

Notes

(1) Mounting surface flat, smooth, and greased, λ_{grease} = 4.0 W/mK, grease thickness 70 µm

(2) Verified by experiment, valid only in certain conditions

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	80	-	-	V
		V_{GS} = 0 V, I_D = 5 mA, T_J = -40 °C	80	-	-	
Static drain to source on-resistance, Q1 (1)	$R_{DS(on)\ Q1}$	V_{GS} = 10 V, I_D = 200 A	-	0.45	0.91	mΩ
Static drain to source on-resistance, Q2 (1)	$R_{DS(on)\ Q2}$	V_{GS} = 10 V, I_D = 200 A	-	0.75	1.21	
Static drain to source on-resistance, Q1	$R_{DS(on)\ Q1}$	V_{GS} = 10 V, I_D = 200 A, T_J = 125 °C	-	0.75	-	mΩ
Static drain to source on-resistance, Q2	$R_{DS(on)\ Q2}$	V_{GS} = 10 V, I_D = 200 A, T_J = 125 °C	-	1.25	-	
Static drain to source on resistance, Q1 module level (2)	$R_{DSQ1module}$	V_{GS} = 10 V, I_D = 200 A	-	1.79	2.35	mΩ
Static drain to source on resistance, Q2 module level (2)	$R_{DSQ2module}$		-	1.79	2.35	
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.3	2.92	4.0	V
		V_{DS} = V_{GS}, I_D = 250 µA, T_J = -40 °C	-	3.34	-	V
Forward transconductance	g_{fs}	V_{DS} = 20 V, I_D = 200 A, V_{GS} = 10 V	-	333	-	S
Drain to source leakage current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V	-	0.1	1	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	50	-	
Internal gate resistance	R_{Gint}		-	1.2	-	Ω
Gate to source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Total gate charge	Q_g	I_D = 80 A, V_{DS} = 48 V, V_{GS} = 0 V / 10 V	-	130	-	nC
Gate to source charge	Q_{gs}		-	39	-	
Gate to drain (“Miller”) charge	Q_{gd}		-	24	-	
Turn-on switching energy (3)	E_{on}	V_{DD} = 52 V, I_D = 250 A, R_{gon} = 54 Ω, R_{goff} = 81 Ω, V_{GS} = 0 V / 13 V	-	0.42	0.7	mJ
Turn-off switching energy (3)	E_{off}		-	2.52	4.0	
Turn-on delay time	$t_{d(on)}$		-	203	-	ns
Rise time	t_r		-	169	-	
Turn-off delay time	$t_{d(off)}$		-	1015	-	
Fall time	t_f		-	256	-	
Turn-on switching energy	E_{on}	T_J = 125 °C, V_{DD} = 52 V, I_D = 250 A, R_{gon} = 54 Ω, R_{goff} = 69 Ω, V_{GS} = 0 V / 13 V	-	0.48	-	mJ
Turn-off switching energy	E_{off}		-	2.28	-	
Turn-on delay time	$t_{d(on)}$		-	186	-	ns
Rise time	t_r		-	175	-	
Turn-off delay time	$t_{d(off)}$		-	900	-	
Fall time	t_f		-	227	-	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 40 V, f = 10 kHz	-	11.2	-	nF
Output capacitance	C_{oss}		-	5.6	-	
Reverse transfer capacitance	C_{rss}		-	30	-	pF

Notes

(1) The difference in $R_{DS(on)}$ values listed in the table refer to the measurement path available inside the module. Q1 and Q2 MOSFETs have the same die size and technology.

(2) Module level $R_{DS(on)}$ values listed in the table refer to the measurement taken on power terminals. High side MOSFET Q1 was measured on terminals 10 to 12, while low side MOSFET Q2 was measured on terminals 12 to 11.

(3) Guaranteed by design, not subjected to production test.

SOURCE-DRAIN ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Diode forward voltage	V_{SD}	I_{SD} = 200 A, V_{GS} = 0 V	-	0.83	1	V
Reverse recovery time	t_{rr}	I_{SD} = 250 A, dI/dt = 2400 A/µs, V_R = 52 V	-	106	-	ns
Reverse recovery charge	Q_{rr}		-	7180	-	nC
Reverse recovery current	I_{RM}		-	107	-	A
Reverse recovery energy	E_{rec}		-	0.3	-	mJ
Reverse recovery time	t_{rr}	T_J = 125 °C, I_{SD} = 250 A, dI/dt = 2400 A/µs, V_R = 52 V	-	100	-	ns
Reverse recovery charge	Q_{rr}		-	6668	-	nC
Reverse recovery current	I_{RM}		-	107	-	A
Reverse recovery energy	E_{rec}		-	0.263	-	mJ

INTERNAL NTC - THERMISTOR SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUE**	**UNITS**
Resistance	R_{25}	T = 25 °C	10 000	Ω
B-value	$B_{25/100}$	$R_2 = R_{25}$ exp. [$B_{25/100}$(1/T2 - 1/(298.15K))]	3625 ± 1 %	K
Operating temperature range at zero power			-40 to +150	°C
Dissipation factor D			3.0	mW/K
Thermal time constant τ			< 4	s

INTERNAL POWER METAL STRIP RESISTOR - ELECTRICAL SPECIFICATION		
POWER RATING (W) P_{70} °C	**VALUE (Ω)**	**TOLERANCE (%)**
8.0	0.0003	± 1.0

INTERNAL POWER METAL STRIP RESISTOR - TECHNICAL SPECIFICATION		
PARAMETER	**UNIT**	**RESISTOR CHARACTERISTICS**
Component temperature coefficient (including terminal) (1)	ppm/K	< 35
Operating temperature range	°C	-65 to 170

Note

(1) Component TCR - total TCR that includes the TCR effects of the resistor element and the copper terminal

INTERNAL CAPACITORS - ELECTRICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**VALUE**	**TOLERANCE (%)**	**UNITS**
Capacitance	C	68	± 10	nF
Voltage	V	100	-	V
Operating temperature range	T_{op}	-55 to +150	-	°C

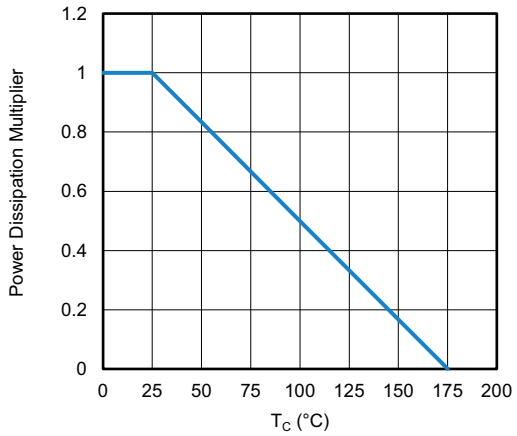


Fig. 1 - Normalized Power Dissipation

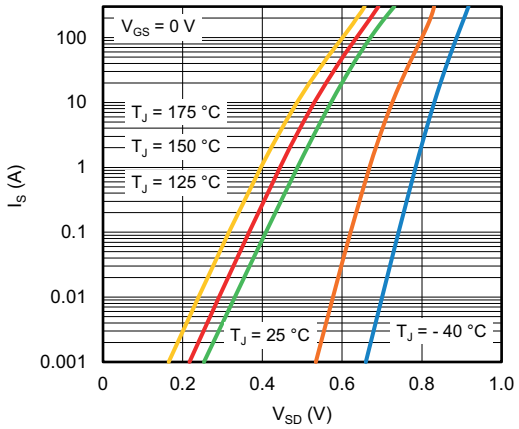


Fig. 4 - Typical Body Diode Source-to-Drain Current Characteristics

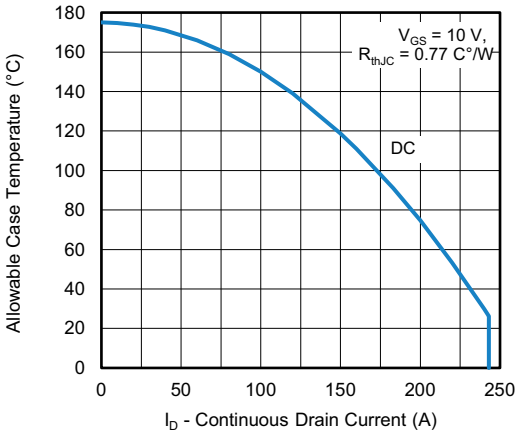


Fig. 2 - Maximum Continuous Drain Current vs. Case Temperature

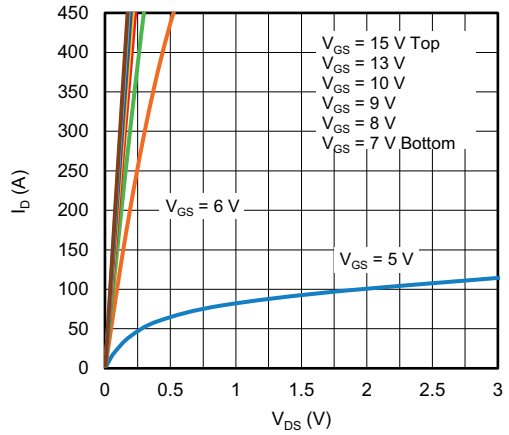


Fig. 5 - Typical Drain to Source Current Output Characteristics at T_J = -40 °C

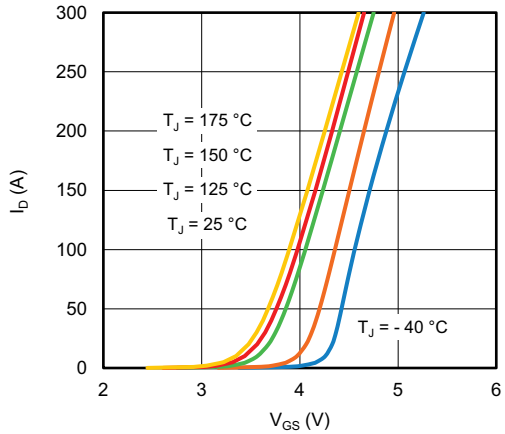


Fig. 3 - Typical Transfer Characteristics

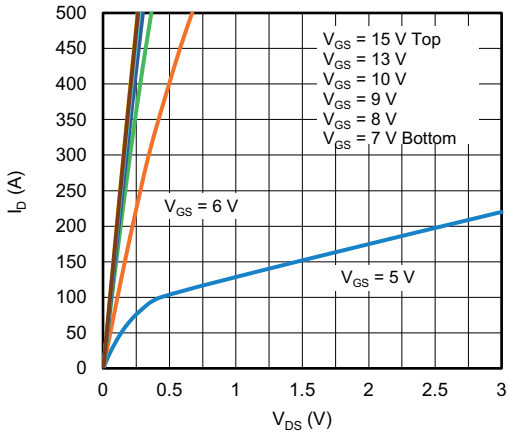


Fig. 6 - Typical Drain to Source Current Output Characteristics at T_J = 25 °C

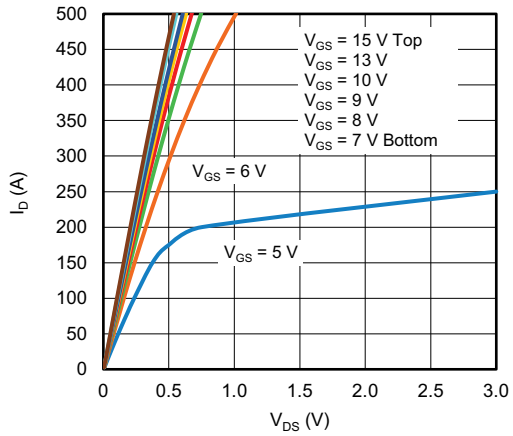


Fig. 7 - Typical Drain to Source Current Output Characteristics at T_J = 175 °C

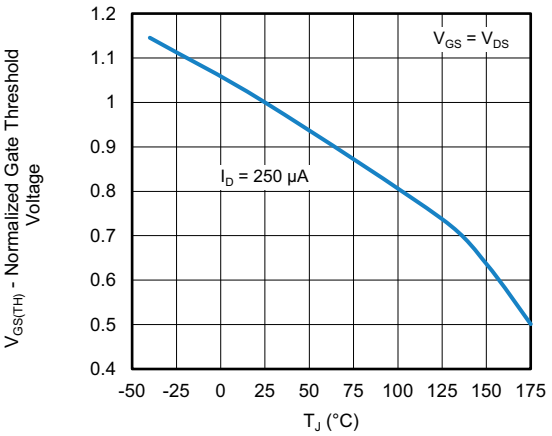


Fig. 10 - Normalized Gate Threshold Voltage vs. Temperature

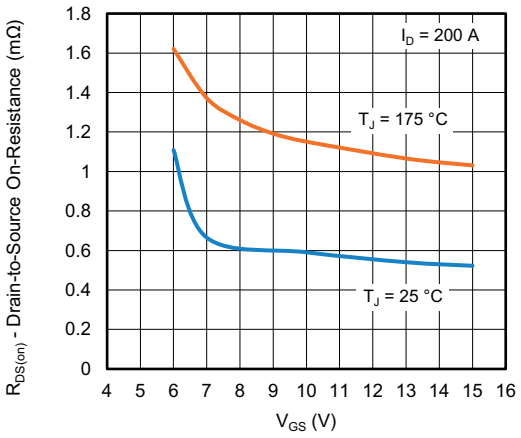


Fig. 8 - Typical Drain-to-Source On-Resistance vs. Gate to Source Voltage

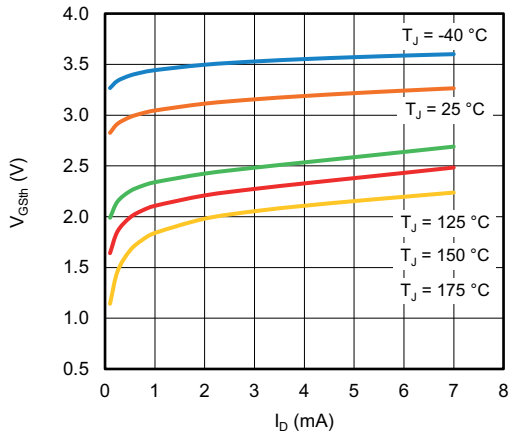


Fig. 11 - Typical Gate Threshold Voltage Characteristics

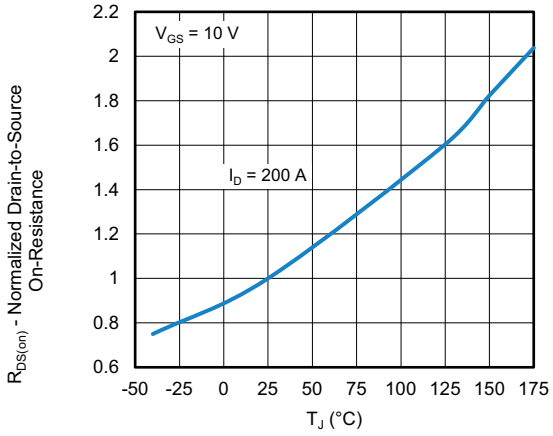


Fig. 9 - Normalized Drain-to-Source On-Resistance vs. Temperature

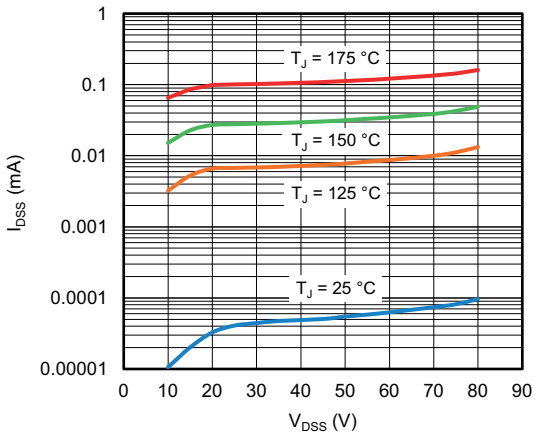


Fig. 12 - Typical Zero Gate Voltage Drain Current

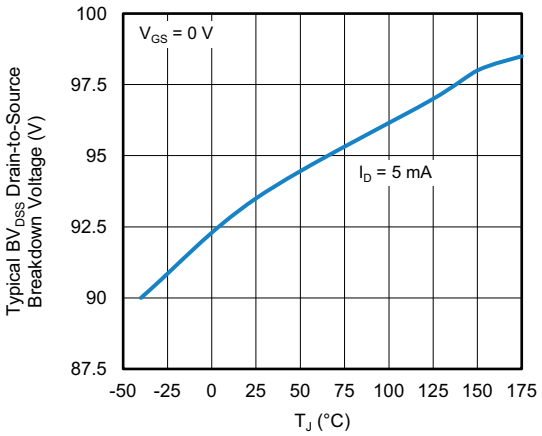


Fig. 13 - Typical Drain to Source Breakdown Voltage vs. Temperature

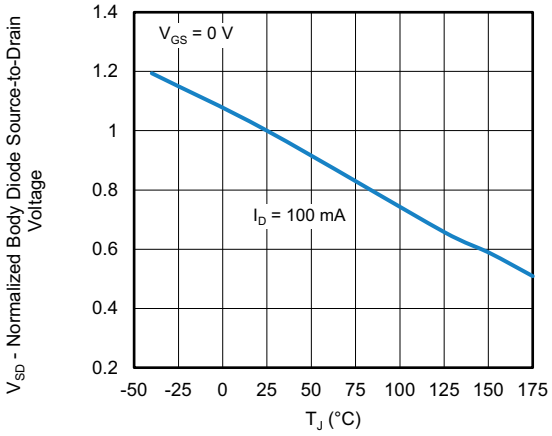


Fig. 16 - Normalized Body Diode Source-to-Drain vs. Temperature

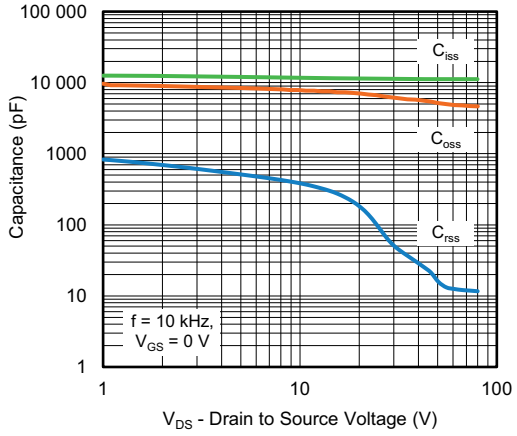


Fig. 14 - Capacitance vs. Drain-to-Source Voltage

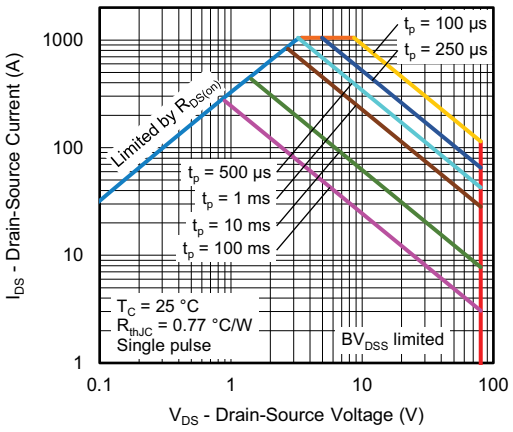


Fig. 17 - Safe Operating Area

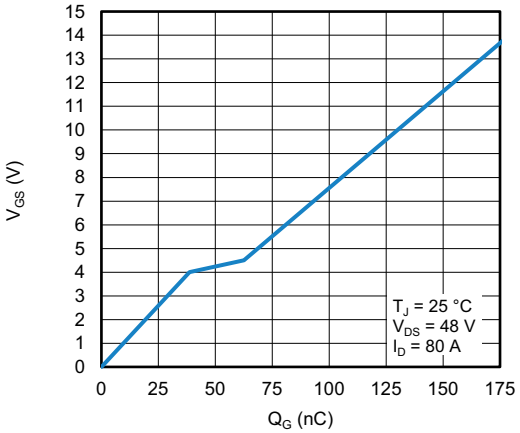


Fig. 15 - Capacitance vs. Drain-to-Source Voltage

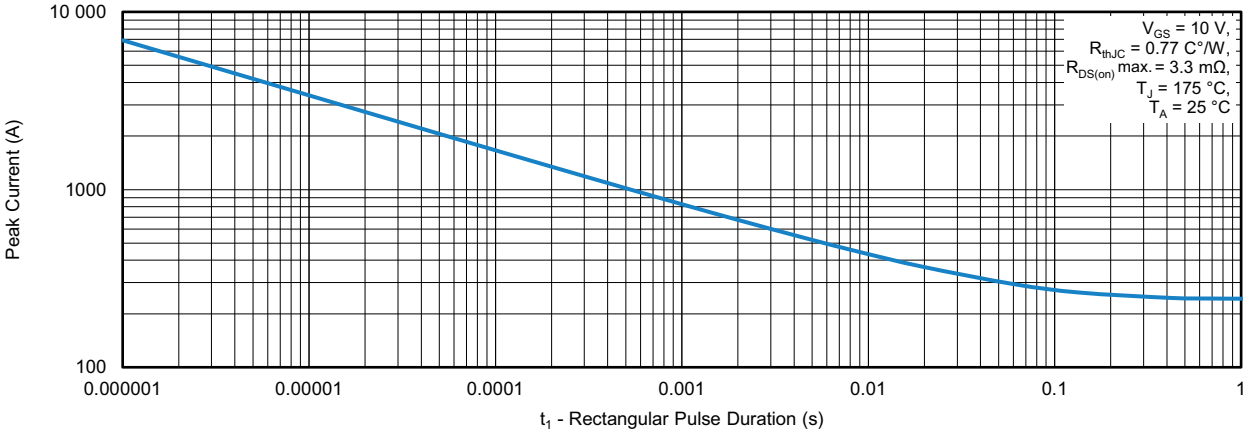


Fig. 18 - Peak Current Capability

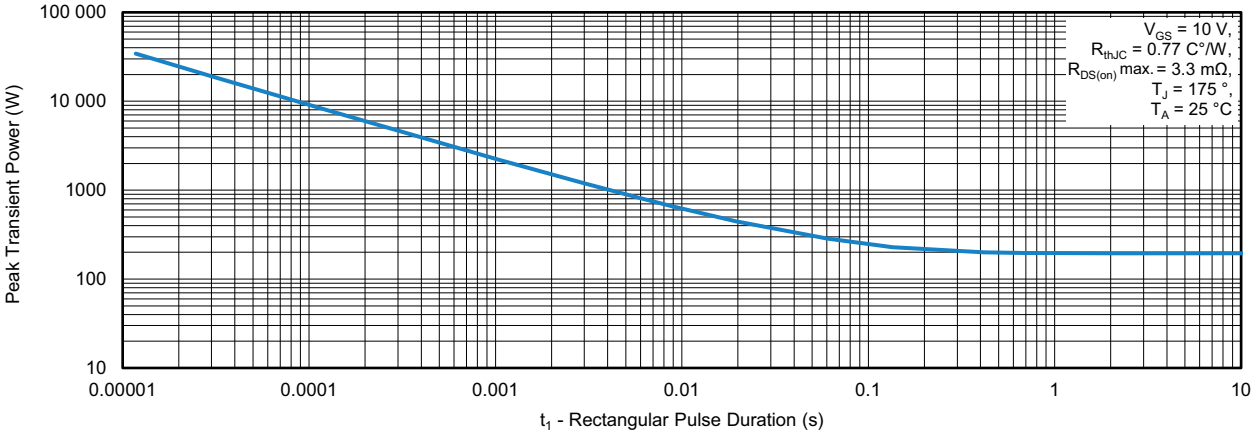


Fig. 19 - Peak Power Capability

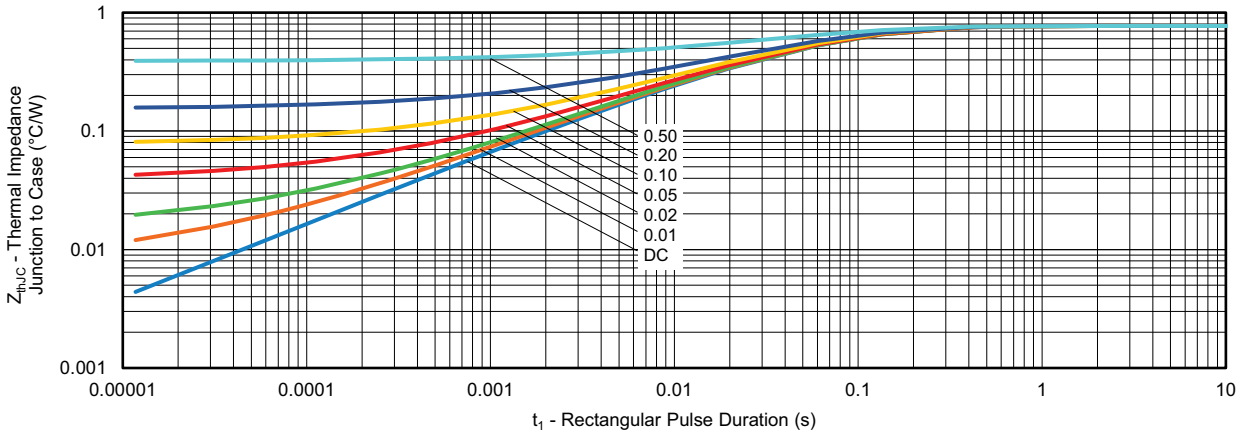


Fig. 20 - Maximum Thermal Impedance Z_{thJC} Characteristics

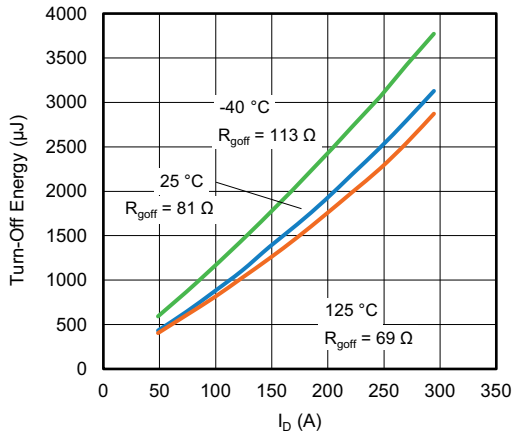


Fig. 21 - Typical Turn-Off Energy Loss vs. I_D
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

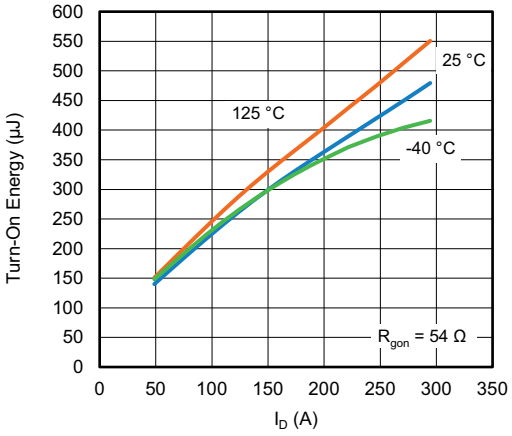


Fig. 22 - Typical Turn-On Energy Loss vs. I_D
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

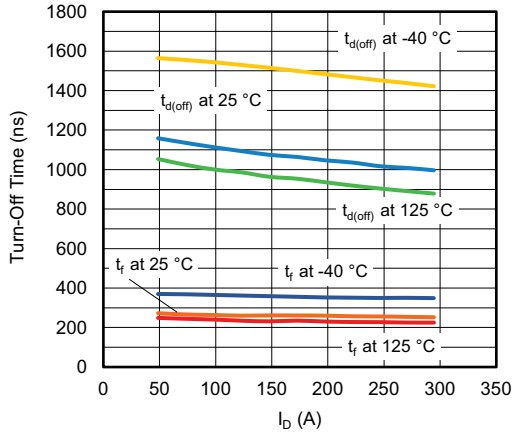


Fig. 23 - Typical Turn-Off Switching Time vs. I_D
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

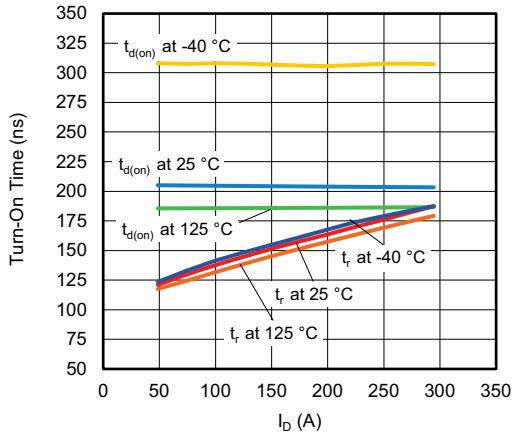


Fig. 24 - Typical Turn-On Switching Time vs. I_D
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

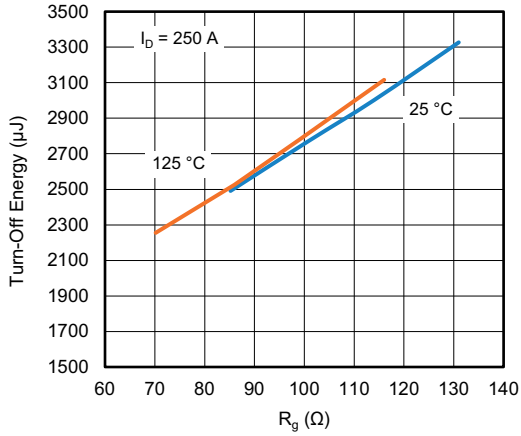


Fig. 25 - Typical Turn-Off Energy Loss vs. R_g
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

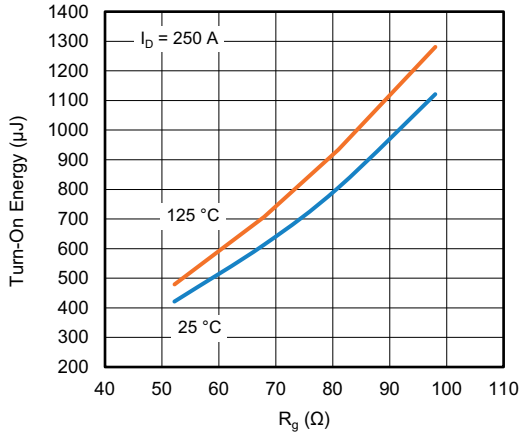


Fig. 26 - Typical Turn-On Energy Loss vs. R_g
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

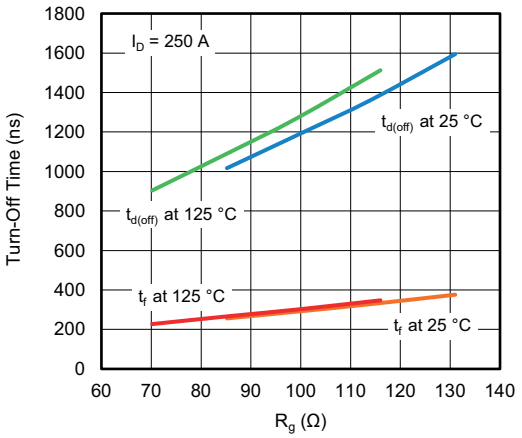


Fig. 27 - Typical Turn-Off Switching Time vs. R_g
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

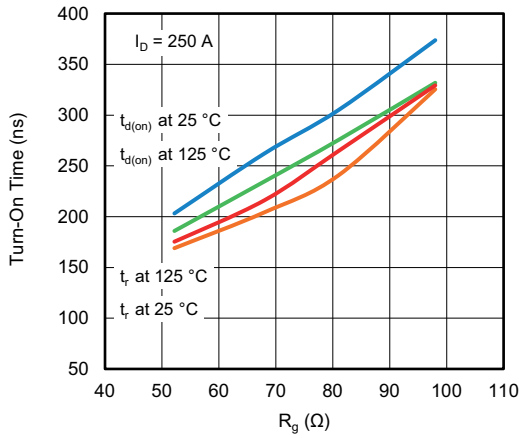


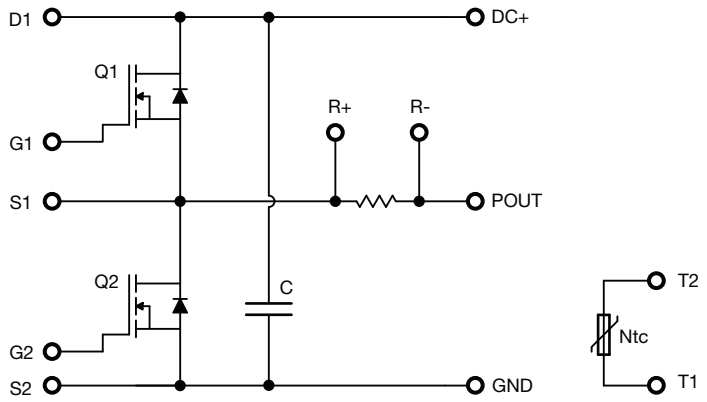
Fig. 28 - Typical Turn-On Switching Time vs. R_g
V_{DD} = 52 V, V_{GS} = 0 V / 13 V

ORDERING INFORMATION TABLE

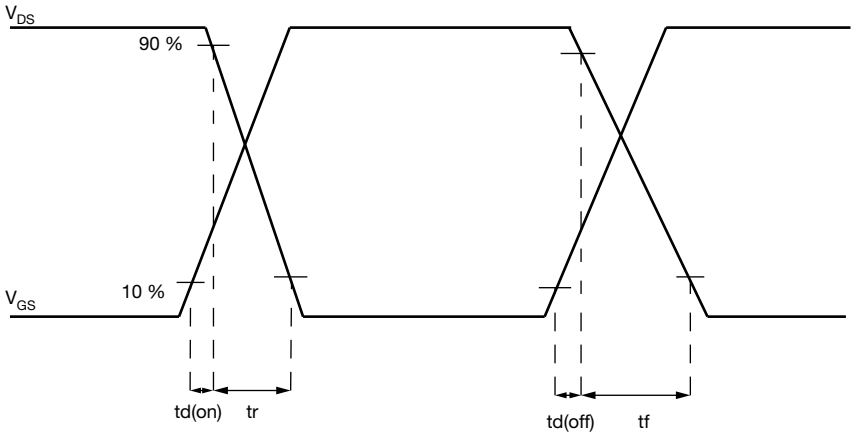
Device code

VS-	HO	T	200	C	080
1	2	3	4	5	6

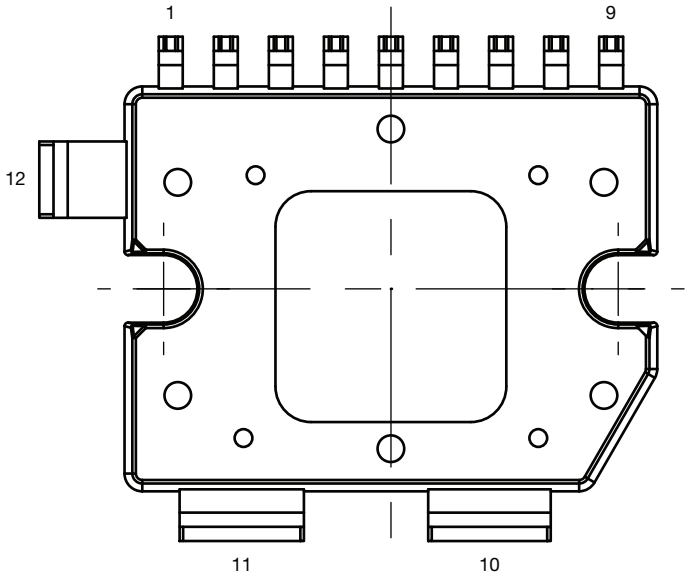
1	-	Vishay Semiconductors product
2	-	Package indicator (HO = FlatPAK HC0)
3	-	Circuit configuration (T = half bridge)
4	-	Current rating (200 = 200 A)
5	-	Switch die technology (C = PowerMOS)
6	-	Voltage rating (080 = 80 V)

CIRCUIT CONFIGURATION		
CIRCUIT	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Half bridge	T	

SWITCHING TIME DEFINITION

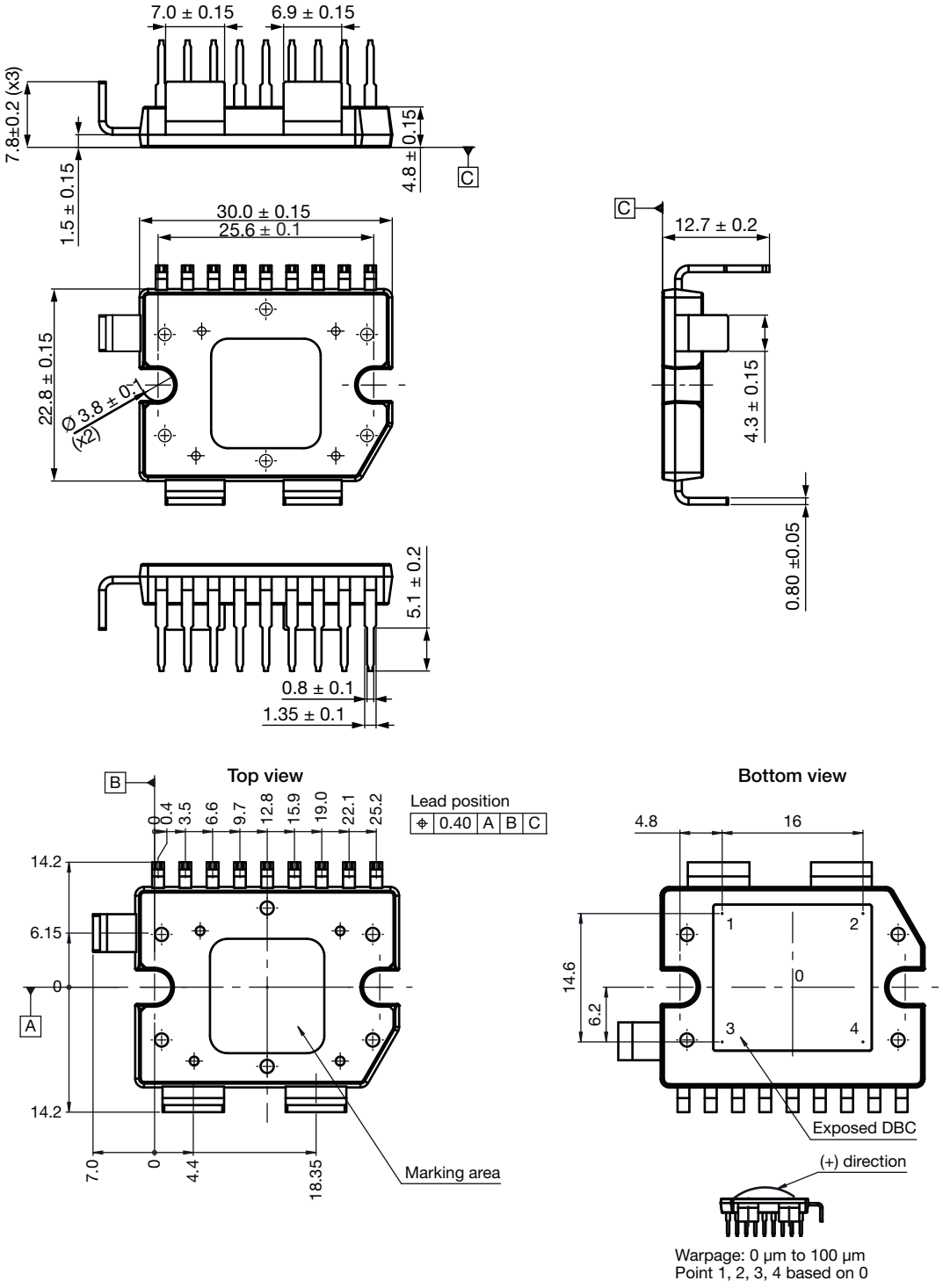


MODULE PIN NUMBERS



PIN TABLE		
PIN ON CIRCUIT	**TERMINAL ON MODULE**	**PIN DESCRIPTION**
G2	1	Q2 low side gate
S2	2	Q2 low side source sense
T1	3	Thermistor 1
T2	4	Thermistor 2
R-	5	Shunt -
R+	6	Shunt +
S1	7	Q1 high side source sense / Q2 low side drain sense
D1	8	Q1 high side drain sense
G1	9	Q1 high side gate
DC+	10	Q1 high side power drain
GND	11	Q2 low side power source
POUT	12	Phase out connection

DIMENSIONS in millimeters



Notes

- Finishing: tin 100 % matt plating 8 µm to 20 µm all over the lead-frame terminals, only except for dumbar cut sections
- Tin plating solderabililty / wettability criteria as per specification J-STD-002E

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