

EMIPAK 2B PressFit Full Bridge Inverter Silicon Carbide MOSFET Power Modules



EMIPAK 2B
(package example)

FEATURES

- Silicon carbide power MOSFET
- Very tight variation of on-resistance vs. temperature
- Slight variation of switching losses with temperature
- Very fast body diode
- PressFit pins technology
- Exposed Al_2O_3 substrate with low thermal resistance
- Low input capacitance
- Low internal inductance
- Easy to drive
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

FULL BRIDGE INVERTER - Q1 to Q6 MOSFET

V_{DSS}	1200 V
$R_{\text{DS(on)}}$ typical at $I_{\text{D}} = 20 \text{ A}$	71 m Ω
I_{D} at $T_{\text{C}} = 80 \text{ }^{\circ}\text{C}$	26 A
Type	Modules - MOSFET
Package	EMIPAK 2B
Circuit configuration	Full bridge

DESCRIPTION

The EMIPAK 2B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

TYPICAL APPLICATIONS

- Solar inverter

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Operating junction temperature	T_{J}		175	$^{\circ}\text{C}$
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	$T_{\text{J}} = 25 \text{ }^{\circ}\text{C}$, all terminals shorted, $f = 50 \text{ Hz}$, $t = 1 \text{ s}$	3500	V
Q1 to Q6 - MOSFET				
Drain to source voltage	V_{DSS}		1200	V
Gate to source voltage	V_{GSS}		-10 / +25	
Pulsed drain current	$I_{\text{DM}}^{(1)}$		90	A
Continuous drain current	I_{D}	$T_{\text{C}} = 25 \text{ }^{\circ}\text{C}$	32	A
		$T_{\text{C}} = 80 \text{ }^{\circ}\text{C}$	26	
		$T_{\text{SINK}} = 80 \text{ }^{\circ}\text{C}$	22	
Power dissipation	P_{D}	$T_{\text{C}} = 25 \text{ }^{\circ}\text{C}$	143	W
		$T_{\text{C}} = 80 \text{ }^{\circ}\text{C}$	90	
Pulsed source current (body diode)	I_{SM}		90	A

Note

⁽¹⁾ Pulse width limited by safe operating area


ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q1 to Q6 - MOSFET						
Drain to source on resistance	$R_{DS(on)}$	$V_{GS} = 20\text{ V}, I_D = 20\text{ A}$	-	71	105	$\text{m}\Omega$
		$V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$	-	79	-	
		$V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	-	81	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1.0\text{ mA}$	1.6	3.6	6.5	V
Temperature coefficient of threshold voltage	$\Delta V_{GS(th)}/\Delta T_J$	$V_{DS} = V_{GS}, I_D = 1.0\text{ mA}$ ($25\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$)	-	-8.3	-	$\text{mV}/^{\circ}\text{C}$
Forward transconductance	g_{fs}	$V_{DS} = 20\text{ V}, I_D = 20\text{ A}$	-	9.5	-	S
Transfer characteristics	V_{GS}	$V_{DS} = 20\text{ V}, I_D = 20\text{ A}$	-	12	-	V
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DD} = 1200\text{ V}$	-	25	230	μA
		$V_{GS} = 0\text{ V}, V_{DD} = 1200\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$	-	50	-	
Gate to source leakage current	I_{GSS}	$V_{GS} = +20\text{ V} / -10\text{ V}, V_{DS} = 0\text{ V}$	-	-	150	nA
Q1 to Q6 - BODY DIODE						
Forward voltage drop	V_{SD}	$I_{SD} = 10\text{ A}; V_{GS} = 0$	-	3.2	-	V

SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Q1 to Q6 - MOSFET						
Total gate charge (turn-on)	Q _g	I _D = 20 A V _{DD} = 800 V V _{GS} = 20 V	-	105	-	nC
Gate to source charge (turn-on)	Q _{gs}		-	16	-	
Gate to drain charge (turn-on)	Q _{gd}		-	40	-	
Turn-on delay time	t _{d(on)}	I _D = 20 A V _{DD} = 600 V V _{GS} = +20 V/-2 V R _g = 4.7 Ω, L = 500 μH	-	41	-	ns
Rise time	t _r		-	29	-	
Turn-off delay time	t _{d(off)}		-	79	-	
Fall time	t _f		-	62	-	
Turn-on delay time	t _{d(on)}	I _D = 20 A V _{DD} = 600 V V _{GS} = +20 V/-2 V R _g = 4.7 Ω, L = 500 μH, T _J = 150 °C	-	41	-	ns
Rise time	t _r		-	30	-	
Turn-off delay time	t _{d(off)}		-	91	-	
Fall time	t _f		-	75	-	
Input capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = 400 V f = 1 MHz	-	1700	-	pF
Output capacitance	C _{oss}		-	130	-	
Reverse transfer capacitance	C _{rss}		-	25	-	
Q1 to Q6 - BODY DIODE						
Diode reverse recovery time	t _{rr}	V _R = 400 V, T _J = 25 °C I _S = 20 A dI/dt = 100 A/μs	-	140	-	ns
Diode reverse recovery current	I _{rr}		-	3.1	-	A
Diode reverse recovery charge	Q _{rr}		-	220	-	nC

**INTERNAL NTC - THERMISTOR SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Resistance	R ₂₅	T _J = 25 °C	22 000 ± 5 %	Ω
	R ₁₅₀	T _J = 150 °C	483.86 ± 5 %	
B constant	B _{25/85}		3800 ± 1 %	K
Operating temperature range at zero power			-40 to +150	°C
Maximum dissipation at 25 °C			210	mW
Dissipation factor	D		3.5	mW/K
Thermal time constant	τ		≈ 10	s

INTERNAL C1 / C3 DC LINK CAPACITOR - ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Capacitance	C		0.047 ± 10 %	μF
Voltage			1000	V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Q1 to Q6 - MOSFET - Junction to case thermal resistance (per switch)	R _{thJC}	-	-	1.05	°C/W
Q1 to Q6 - MOSFET - Case to sink thermal resistance (per switch)	R _{thCS}	-	0.55	-	
Mounting torque (M4) ⁽¹⁾		2	-	3	Nm
Weight		-	45	-	g

Note

⁽¹⁾ See application note for further suggestion on mounting operation: www.vishay.com/doc?95580.

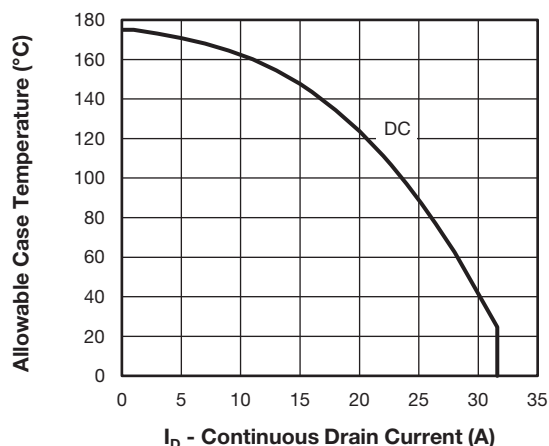


Fig. 1 - Maximum Continuous Drain Current vs. Case Temperature

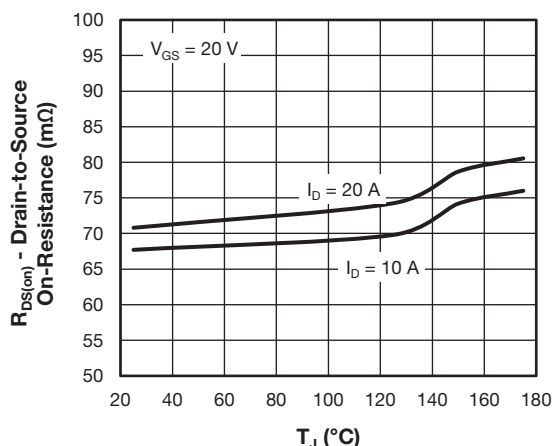


Fig. 4 - Typical Drain-to-Source On-Resistance vs. Temperature

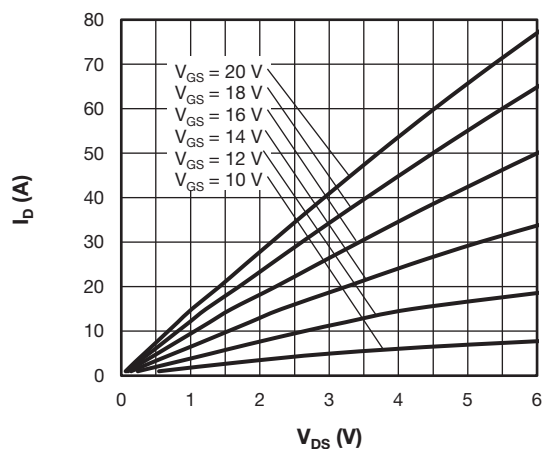


Fig. 2 - Typical Drain-to-Source Current Output Characteristics at $T_J = 25$ °C

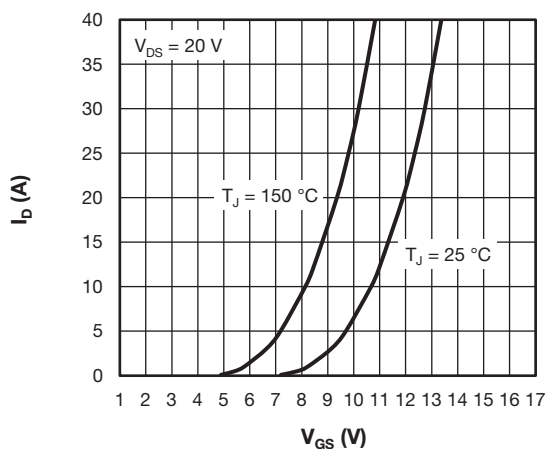


Fig. 5 - Typical Transfer Characteristics

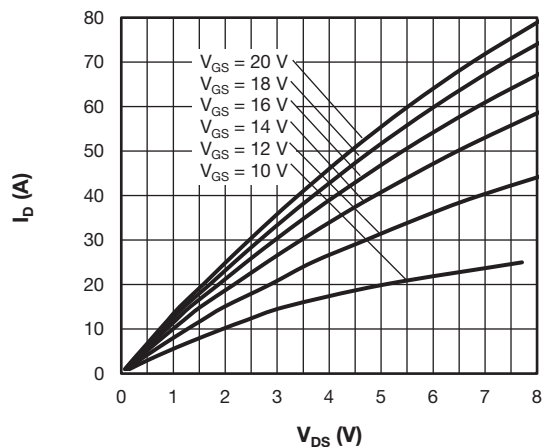


Fig. 3 - Typical Drain-to-Source Current Output Characteristics at $T_J = 150$ °C

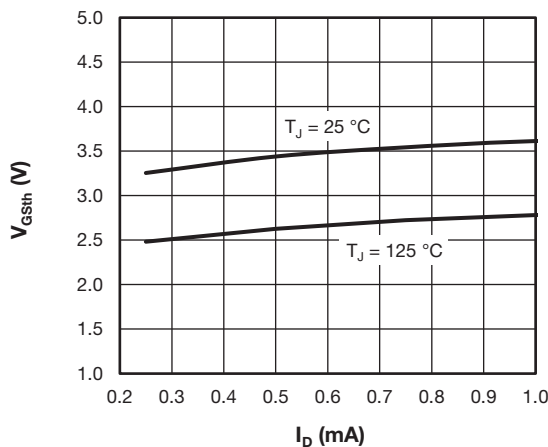


Fig. 6 - Typical Gate Threshold Voltage Characteristics

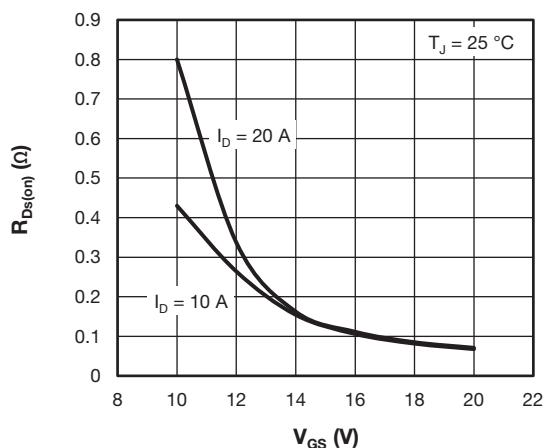


Fig. 7 - Typical Drain-State Resistance vs. Gate-to-Source Voltage

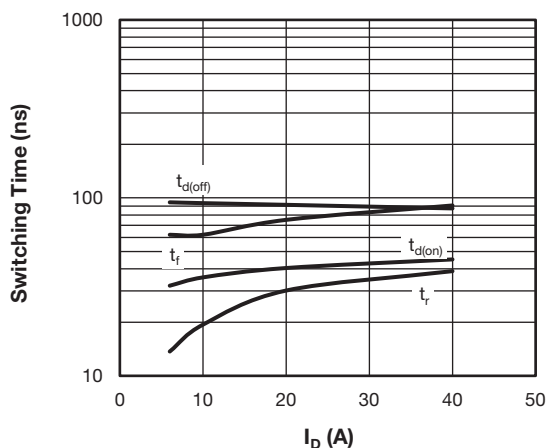


Fig. 10 - Typical Switching Time vs. I_D
 $T_J = 150\text{ }^{\circ}\text{C}$, $V_{DD} = 600\text{ V}$, $R_g = 4.7\text{ }\Omega$, $V_{GS} = +20\text{ V} / -2\text{ V}$, $L = 500\text{ }\mu\text{H}$

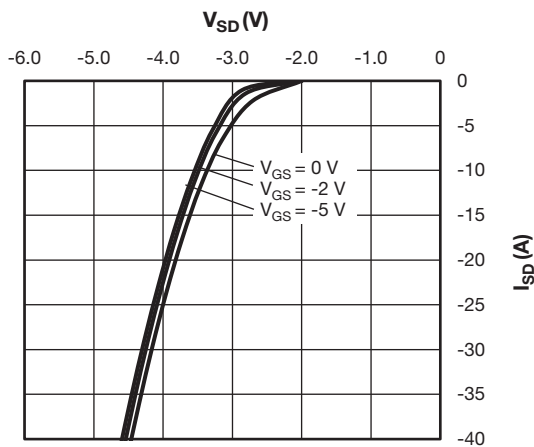


Fig. 8 - Typical Body Diode Source-to-Drain Current Characteristics
at $T_J = 25\text{ }^{\circ}\text{C}$

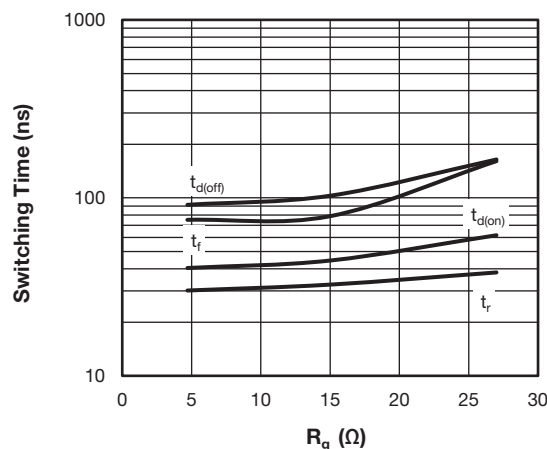


Fig. 11 - Typical Switching Time vs. R_g
 $T_J = 150\text{ }^{\circ}\text{C}$, $V_{DD} = 600\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = +20\text{ V} / -2\text{ V}$, $L = 500\text{ }\mu\text{H}$

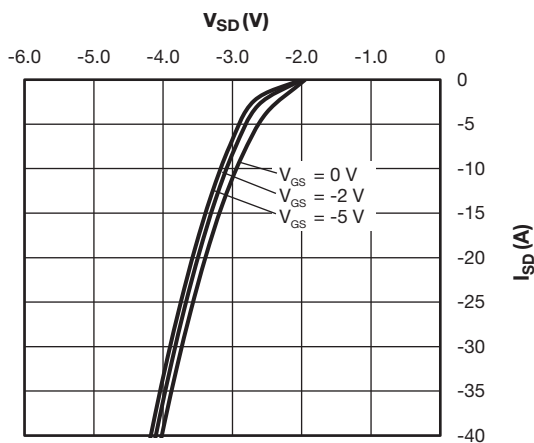


Fig. 9 - Typical Body Diode Source-to-Drain Current Characteristics
at $T_J = 150\text{ }^{\circ}\text{C}$

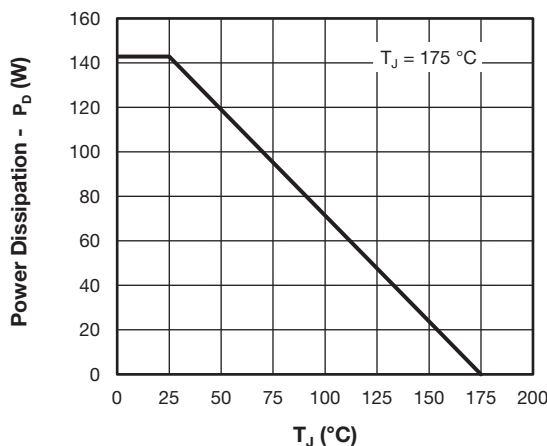


Fig. 12 - Power Dissipation Curve

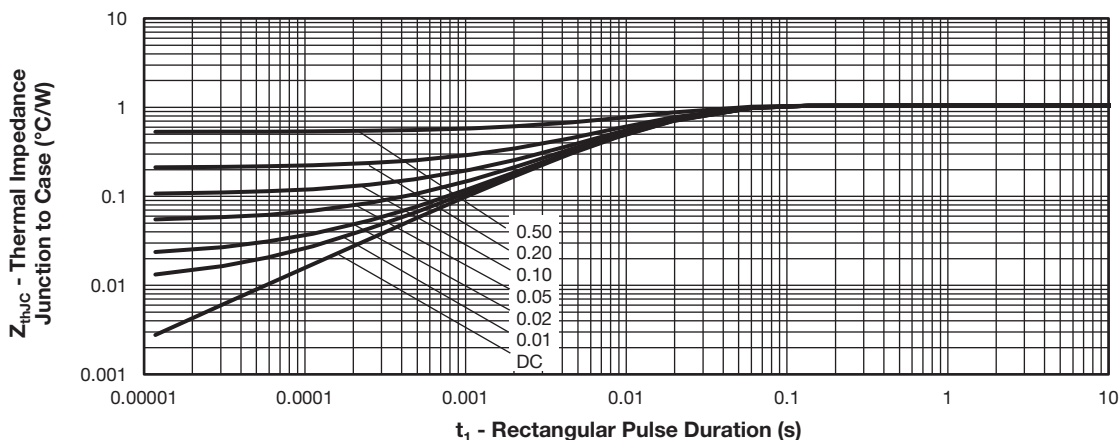


Fig. 13 - Maximum Thermal Impedance Junction-to-Case Characteristics

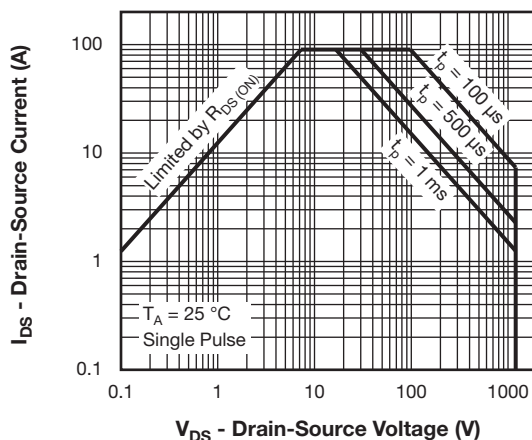


Fig. 14 - Safe Operating Area

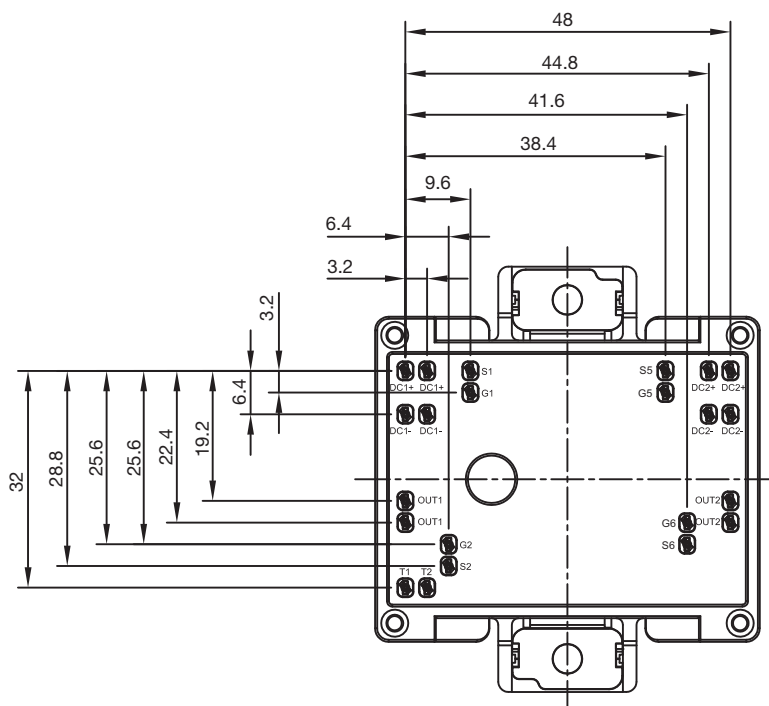
ORDERING INFORMATION TABLE

Device code	VS-	ET	Y	020	P	120	F
	①	②	③	④	⑤	⑥	⑦
①	-	Vishay Semiconductors product					
②	-	Package indicator (ET = EMIPAK 2B)					
③	-	Circuit configuration (Y = full bridge inverter)					
④	-	Current rating (020 = 20 A)					
⑤	-	Switch die technology					
⑥	-	Voltage rating (120 = 1200 V)					
⑦	-	Diode die technology					



CIRCUIT CONFIGURATION		
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Full bridge inverter	Y	

PACKAGE

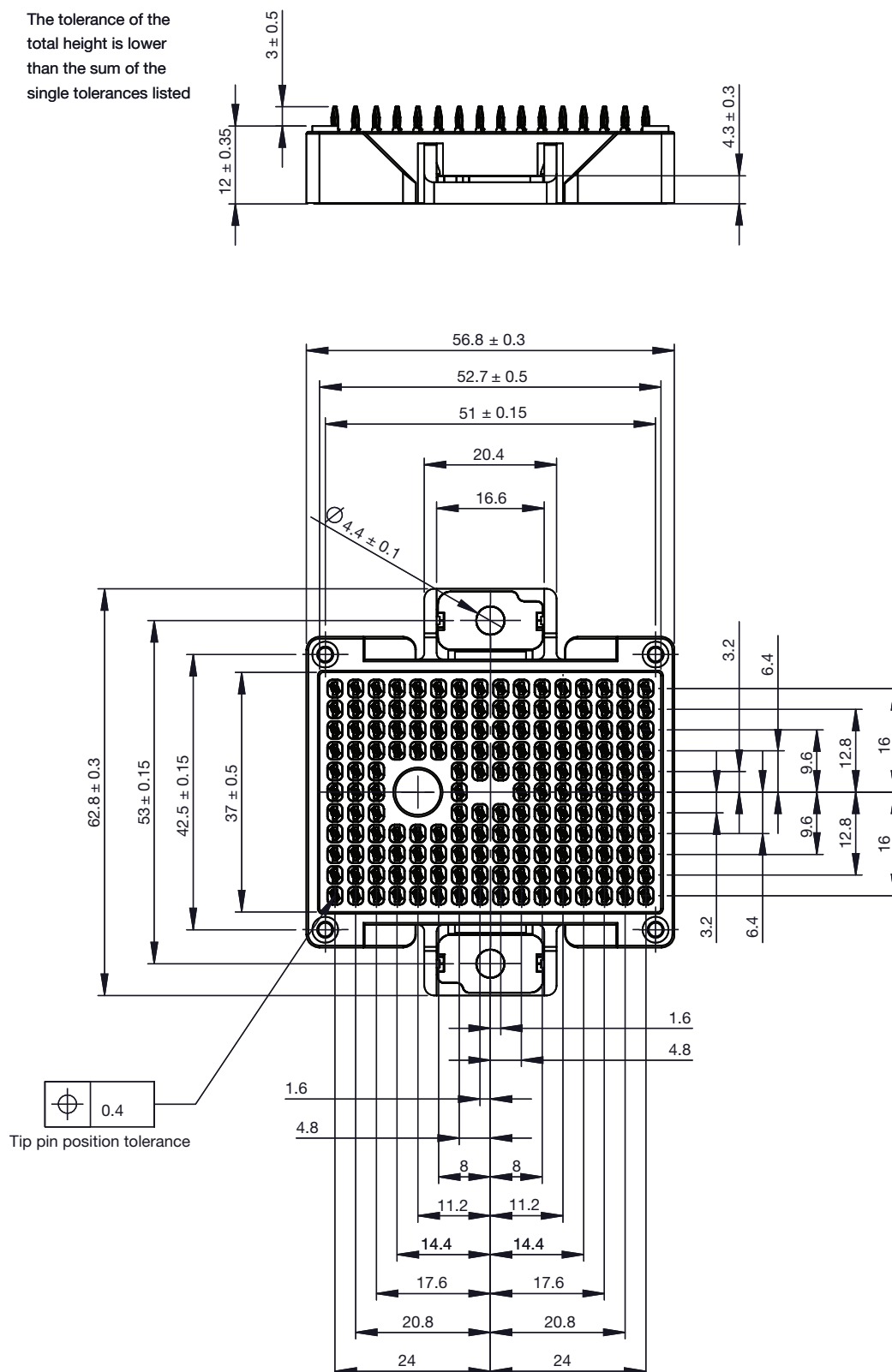


LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95559

EMIPAK 2B

DIMENSIONS in millimeters

The tolerance of the total height is lower than the sum of the single tolerances listed





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