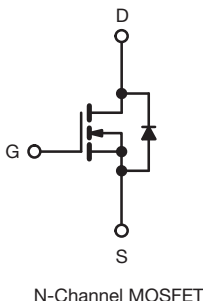


E Series Power MOSFET

Thin-Lead TO-220 FULLPAK



FEATURES

- Low figure-of-merit (FOM): $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Hard switched topologies
- Power factor correction power supplies (PFC)
- Switch mode power supplies (SMPS)
- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (Ω) at 25 °C	$V_{GS} = 10$ V	0.145
Q_g max. (nC)	86	
Q_{gs} (nC)	14	
Q_{gd} (nC)	25	
Configuration	Single	

ORDERING INFORMATION

Package	Thin-Lead TO-220 FULLPAK
Lead (Pb)-free	SiHA25N50E-E3
Lead (Pb)-free and halogen-free	SiHA25N50E-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C) ^e	V_{GS} at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current ^a	I_{DM}	50	
Linear derating factor		0.2	W/°C
Single pulse avalanche energy ^b	E_{AS}	273	mJ
Maximum power dissipation	P_D	35	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	dV/dt	$V_{DS} = 0$ V to 80 % V_{DS}	V/ns
Reverse diode dV/dt ^d			
Soldering recommendations (peak temperature) ^c	for 10 s	300	°C
Mounting torque	M3 screw	0.6	Nm

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.4$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature

THERMAL RESISTANCE RATINGS

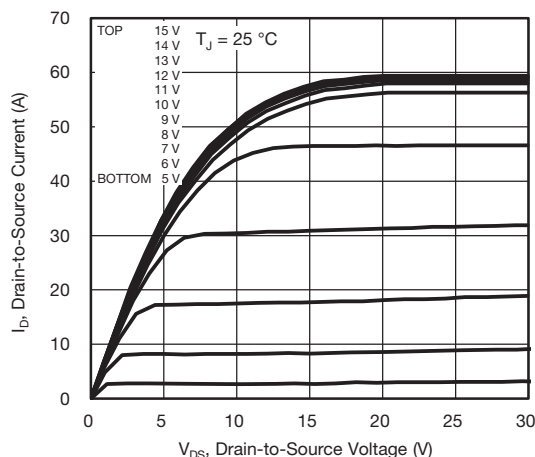
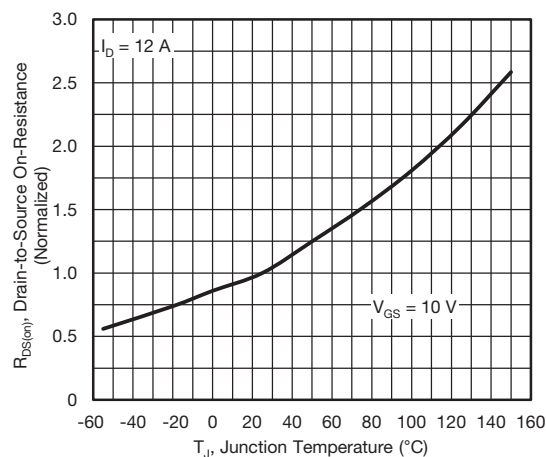
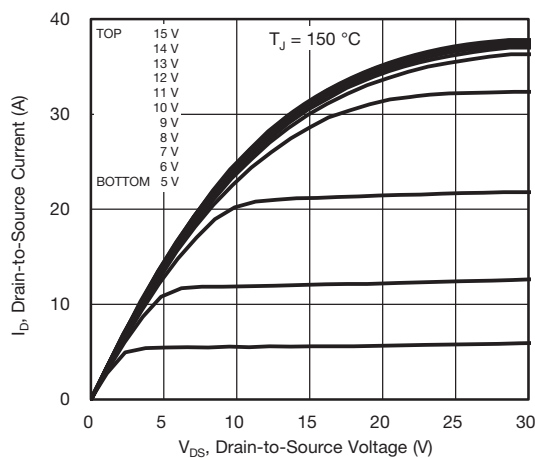
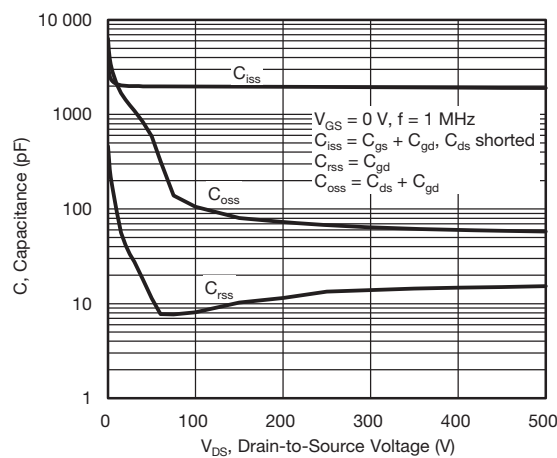
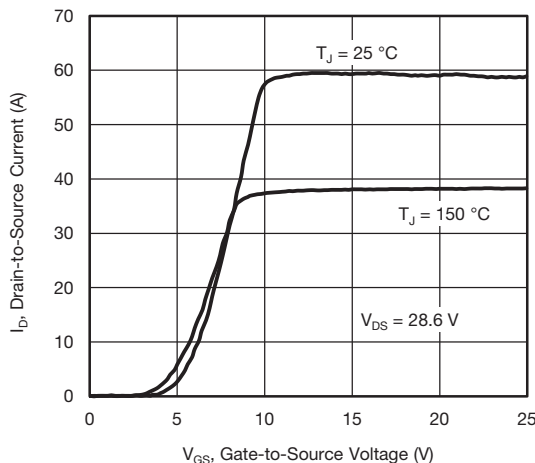
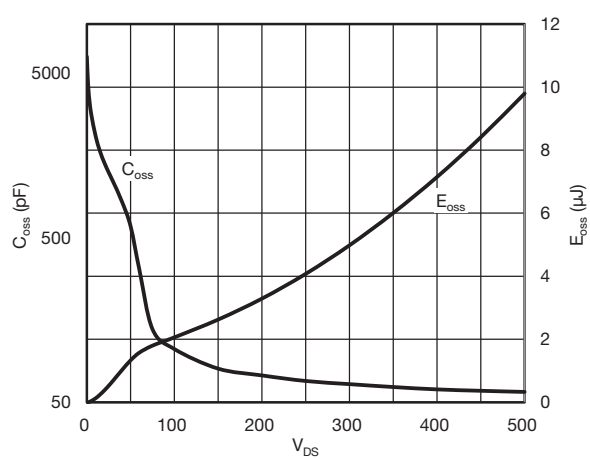
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.6	

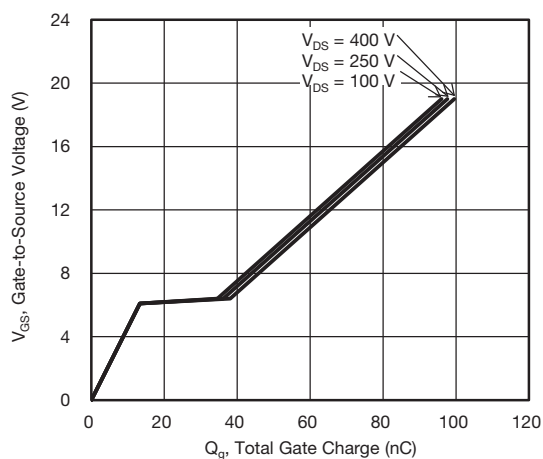
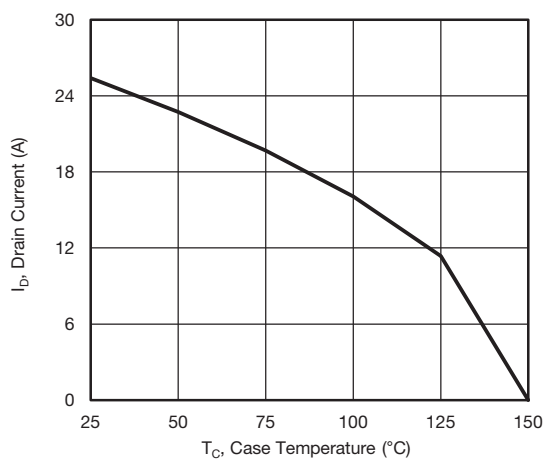
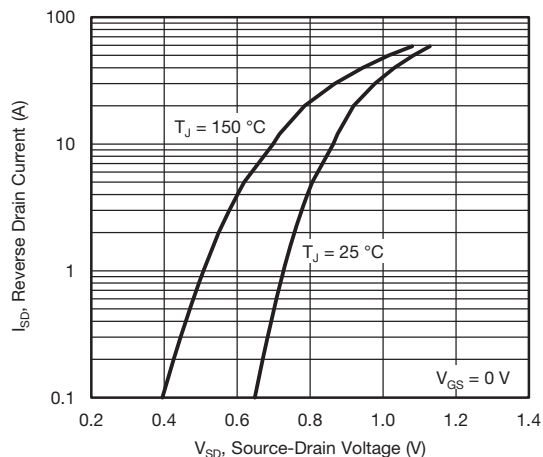
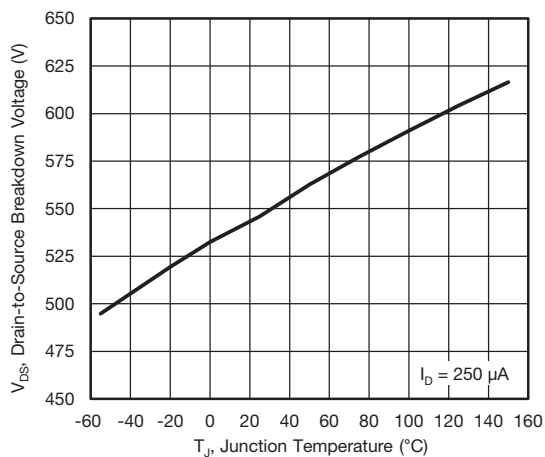
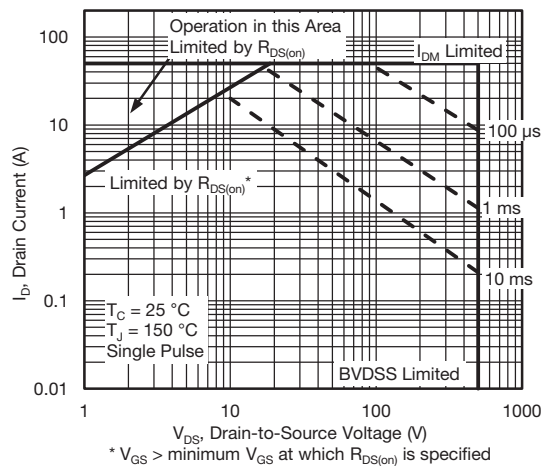


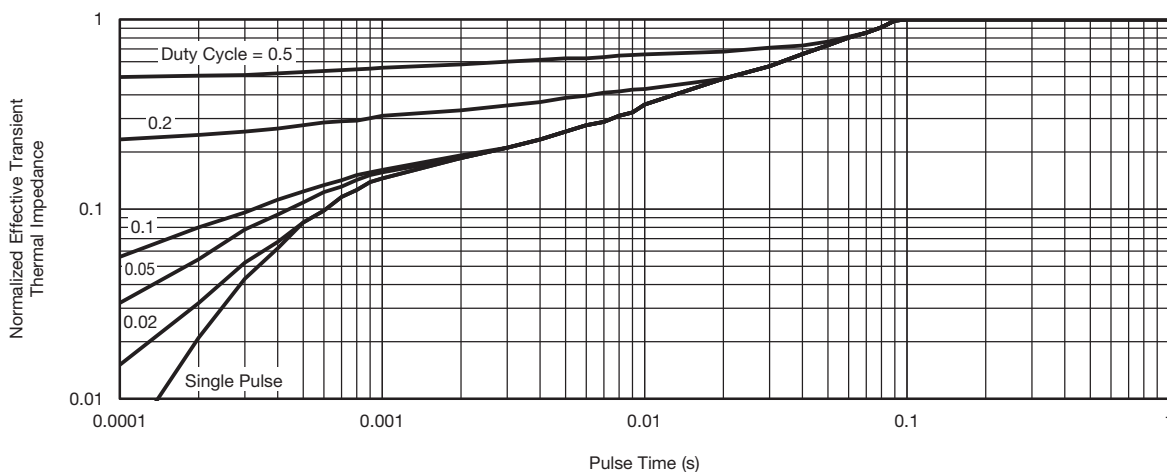
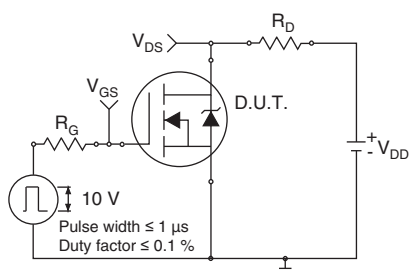
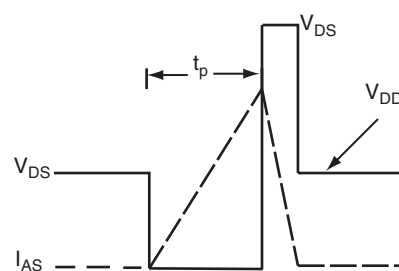
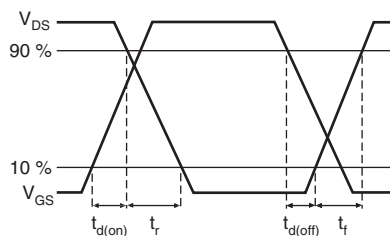
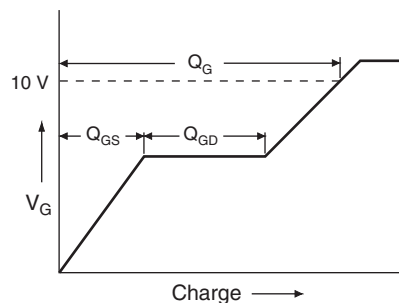
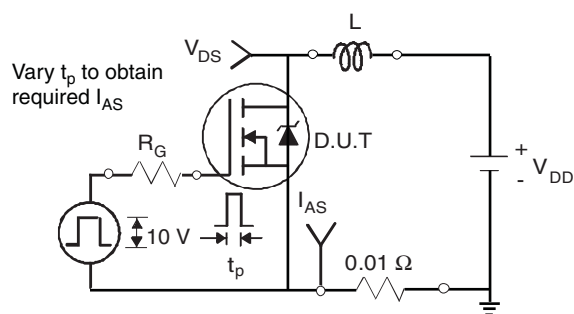
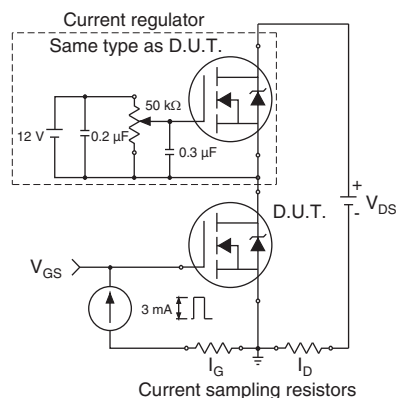
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.59	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C		-	-	25	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A	-	0.125	0.145	Ω
Forward transconductance	g _{fs}	V _{DS} = 30 V, I _D = 12 A		-	6.6	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	1980	-	pF
Output capacitance	C _{Oss}			-	105	-	
Reverse transfer capacitance	C _{rss}			-	8	-	
Effective output capacitance, energy related ^a	C _{O(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	105	-	pF
Effective output capacitance, time related ^b	C _{O(tr)}			-	285	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 12 A, V _{DS} = 400 V	-	57	86	nC
Gate-source charge	Q _{gs}			-	14	-	
Gate-drain charge	Q _{gd}			-	25	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 400 V, I _D = 12 A R _g = 9.1 Ω, V _{GS} = 10 V		-	19	38	ns
Rise time	t _r			-	36	72	
Turn-off delay time	t _{d(off)}			-	57	86	
Fall time	t _f			-	29	58	
Gate input resistance	R _g	f = 1 MHz, open drain		-	0.56	-	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	12	A
Pulsed diode forward current	I _{SM}			-	-	50	
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 16.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}	T _J = 25 °C, I _F = I _S , dI/dt = 100 A/μs, V _R = 25 V		-	338	-	ns
Reverse recovery charge	Q _{rr}			-	5.3	-	μC
Reverse recovery current	I _{RRM}			-	29	-	A

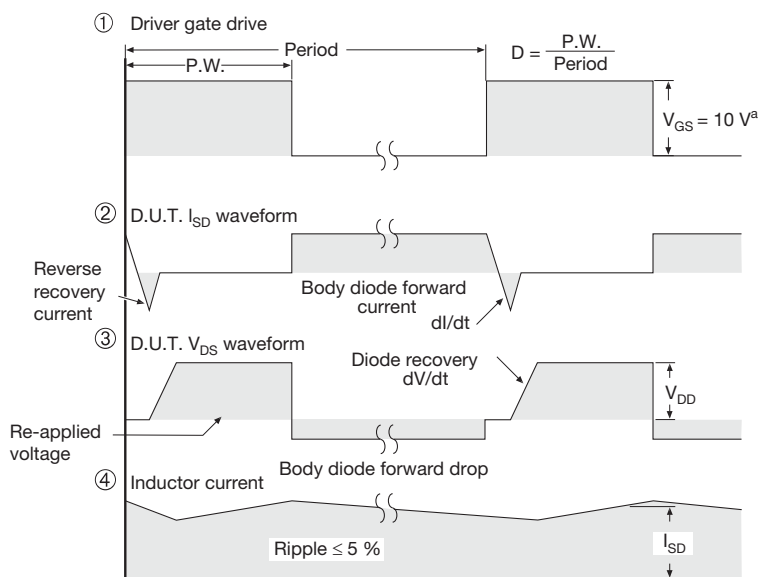
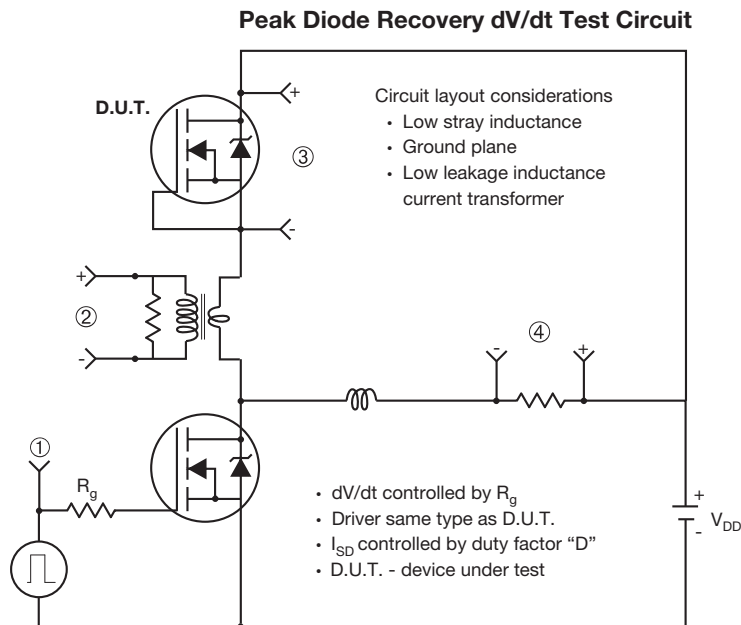
Notes

- a. C_{oss(er)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. C_{oss(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit



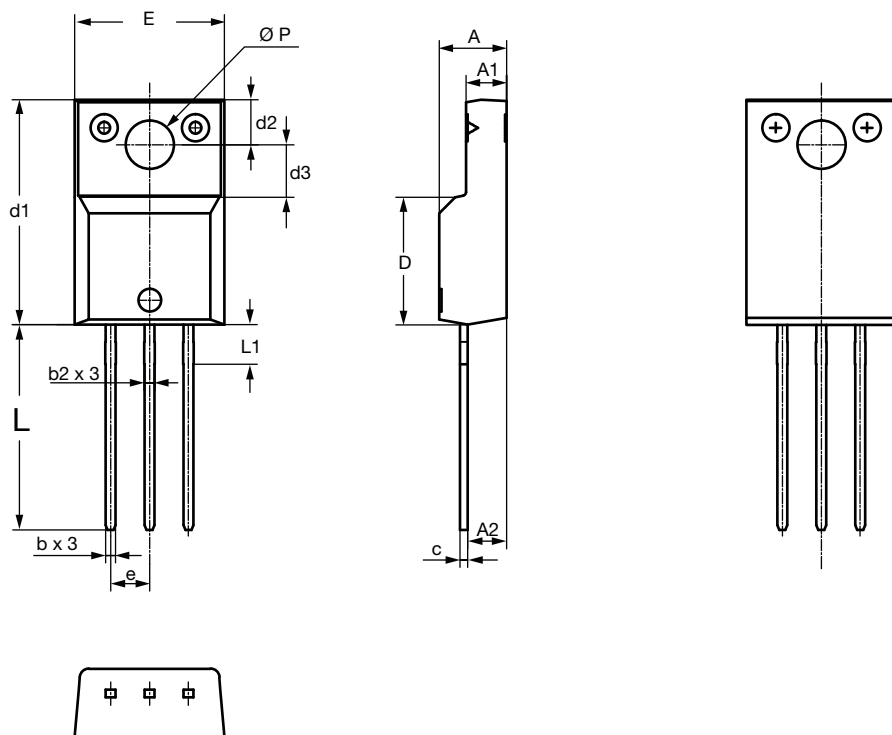
Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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TO-220 FULLPAK Thin Lead



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.30	4.70	0.169	0.185
A1	2.50	2.90	0.098	0.114
A2	2.40	2.80	0.094	0.110
b	0.60	0.80	0.024	0.031
b2	0.60	0.90	0.024	0.035
c	-	0.60	-	0.024
D	8.30	8.70	0.327	0.342
d1	14.70	15.30	0.579	0.602
d2	2.90	3.10	0.114	0.122
d3	3.30	3.70	0.130	0.146
E	9.70	10.30	0.382	0.406
e	2.50	2.70	0.098	0.106
L	13.40	13.80	0.528	0.543
L1	1.00	2.80	0.039	0.110
Ø P	3.00	3.40	0.118	0.134
ECN: E20-0684-Rev. D, 28-Dec-2020 DWG: 6021				



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