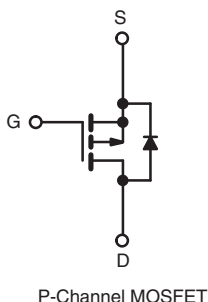
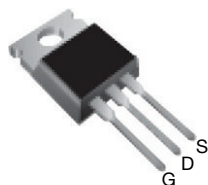


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-50	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	0.28
Q_g max. (nC)	26	
Q_{gs} (nC)	6.2	
Q_{gd} (nC)	8.6	
Configuration	Single	

TO-220AB


FEATURES

- P-channel versatility
- Compact plastic package
- Fast switching
- Low drive current
- Ease of paralleling
- Excellent temperature stability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the power MOSFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-channel power MOSFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-channel power MOSFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-channel power MOSFETs are intended for use in power stages where complementary symmetry with N-channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9Z20PbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-50	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	-39	
Linear Derating Factor		0.32	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM}	-39	A
Unclamped Inductive Current (Avalanche current)	I_L	-2.2	A
Maximum Power Dissipation	P_D	40	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering Recommendations (Peak temperature) ^c	for 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
- $V_{DD} = -25$ V, starting $T_J = 25^\circ\text{C}$, $L = 100\ \mu\text{H}$, $R_g = 25\ \Omega$
- 0.063" (1.6 mm) from case.

**THERMAL RESISTANCE RATINGS**

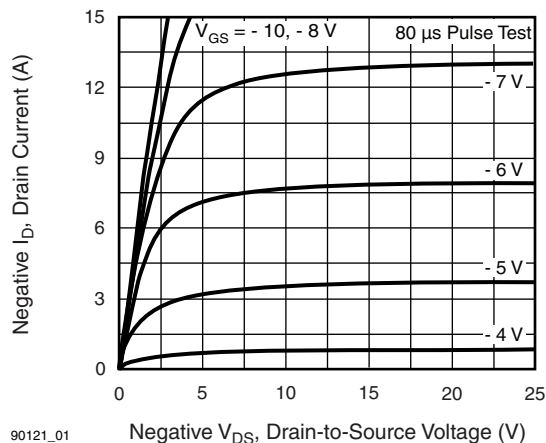
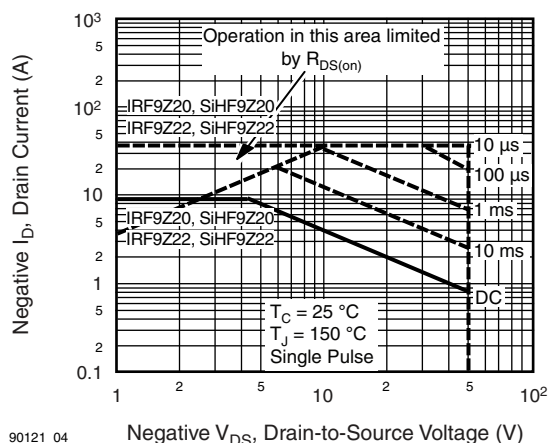
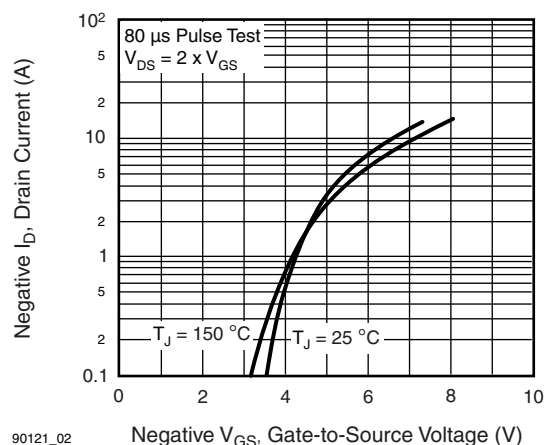
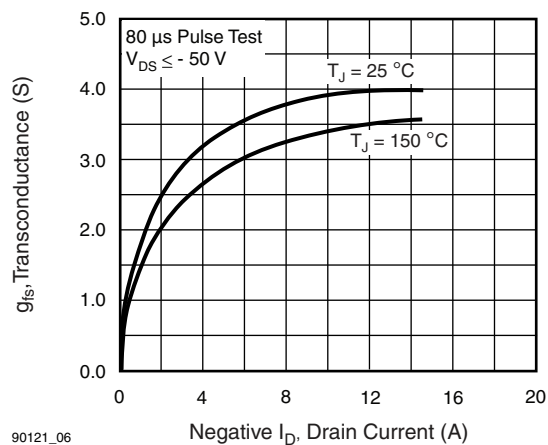
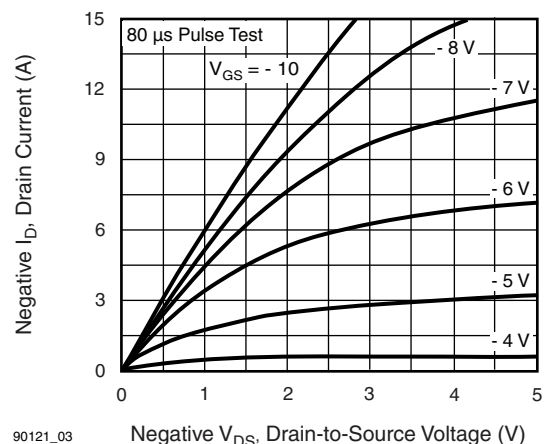
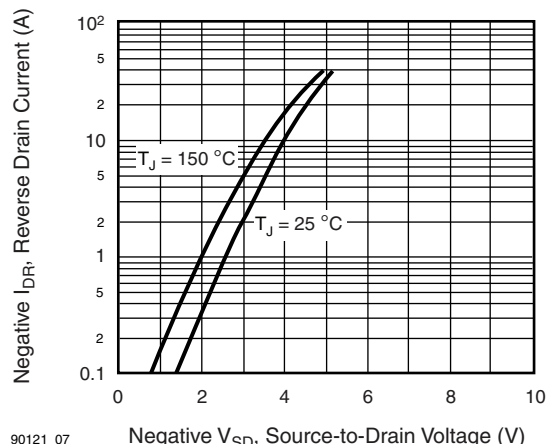
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	80	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	1.0	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

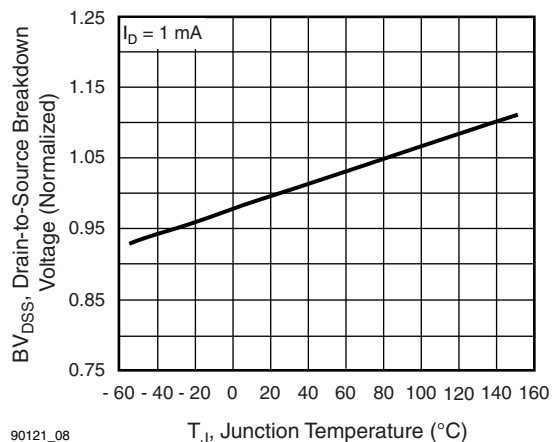
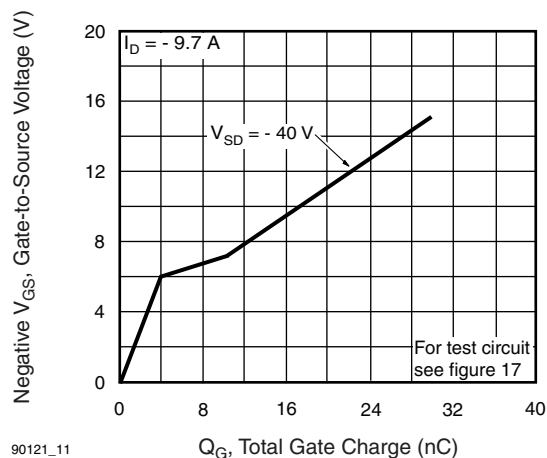
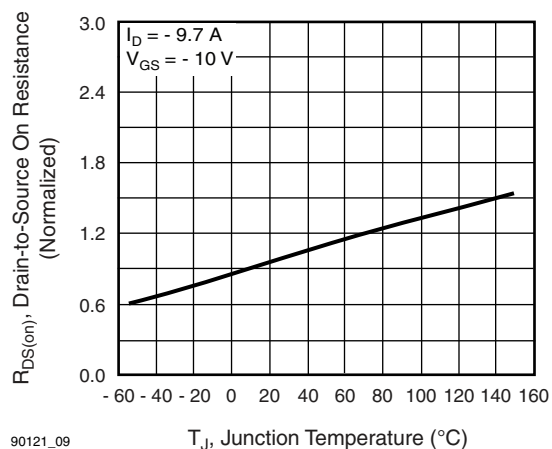
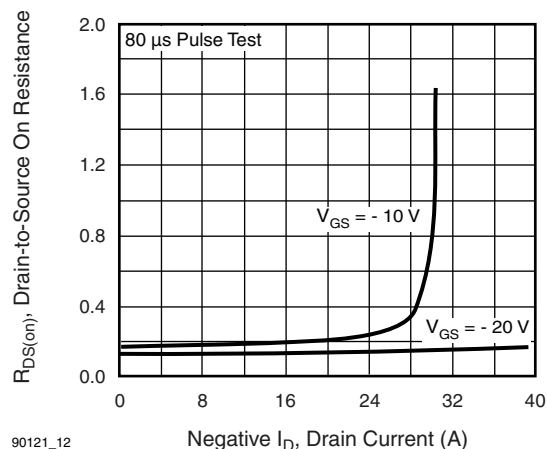
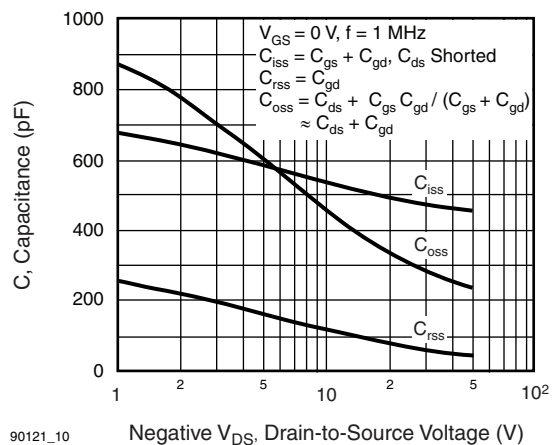
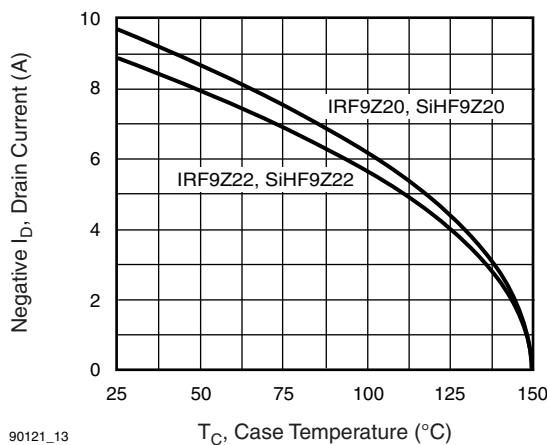
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

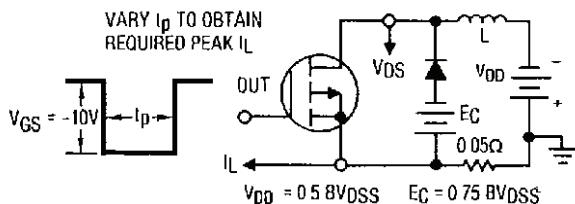
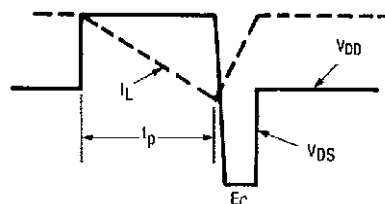
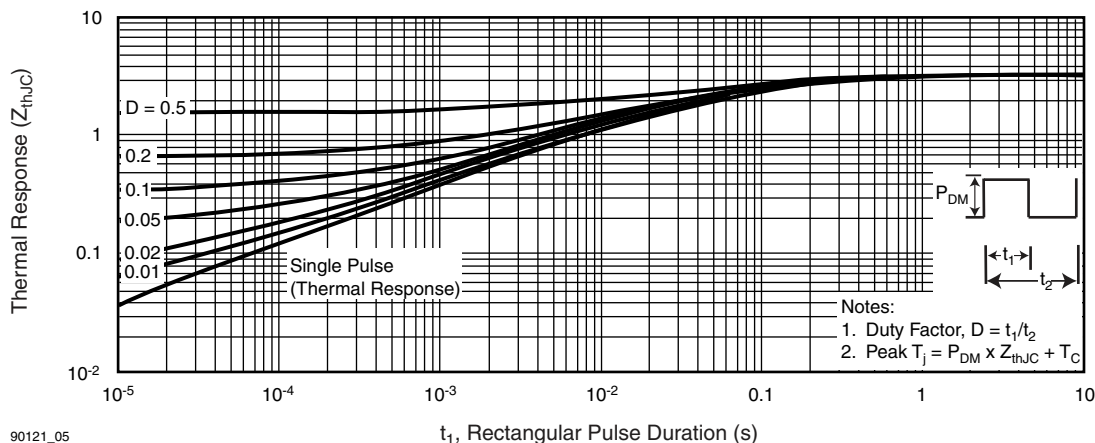
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$		-50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{max. rating}$, $V_{GS} = 0\text{ V}$		-	-	-250	μA
		$V_{DS} = \text{max. rating} \times 0,8$, $V_{GS} = 0\text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	-1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -5.6\text{ A}^b$	-	0.20	0.28	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 2 \times V_{GS}$, $I_{DS} = -5.6\text{ A}^b$		2.3	3.5	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = -25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 9		-	480	-	pF
Output Capacitance	C_{oss}			-	320	-	
Reverse Transfer Capacitance	C_{rss}			-	58	-	
Total Gate Charge	Q_g	$V_{GS} = -10\text{ V}$	$I_D = -9.7\text{ A}$, $V_{DS} = -0.8\text{ max. rating}$, see fig. 17	-	17	26	nC
Gate-Source Charge	Q_{gs}			-	4.1	6.2	
Gate-Drain Charge	Q_{gd}			-	5.7	8.6	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -25\text{ V}$, $I_D = -9.7\text{ A}$, $R_g = 18\text{ }\Omega$, $R_D = 2.4\text{ }\Omega$, see fig. 16 (MOSFET switching times are essentially independent of operating temperature)		-	8.2	12	ns
Rise Time	t_r			-	57	86	
Turn-Off Delay Time	$t_{d(off)}$			-	12	18	
Fall Time	t_f			-	25	38	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-9.7	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-39	
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = -9.7\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	-6.3	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = -9.7\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		56	110	280	ns
Body Diode Reverse Recovery Charge	Q_{rr}			0.17	0.34	0.85	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

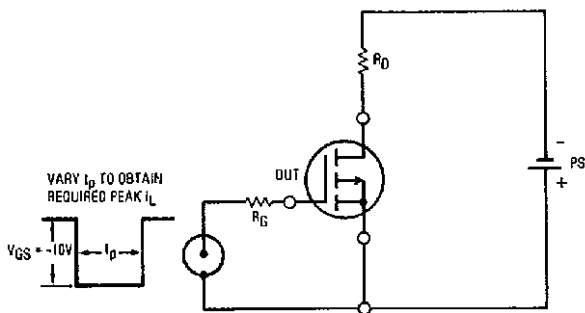
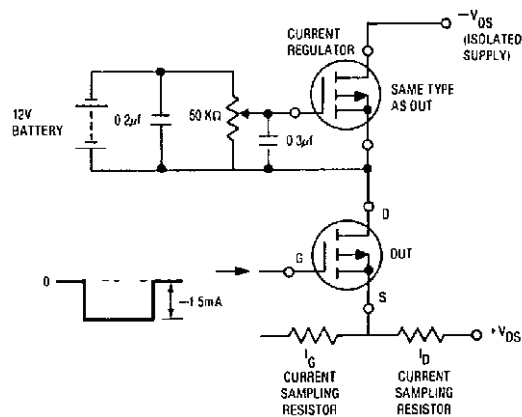
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Maximum Safe Operating Area

Fig. 2 - Typical Transfer Characteristics

Fig. 5 - Typical Transconductance vs. Drain Current

Fig. 3 - Typical Saturation Characteristics

Fig. 6 - Typical Source-Drain Diode Forward Voltage


Fig. 7 - Breakdown Voltage vs. Temperature

Fig. 10 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 8 - Normalized On-Resistance vs. Temperature

Fig. 11 - Typical On-Resistance vs. Drain Current

Fig. 9 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 12 - Maximum Drain Current vs. Case Temperature


Fig. 13a - Unclamped Inductive Test Circuit

Fig. 13b - Unclamped Inductive Load Test Waveforms


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Fig. 14 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

Fig. 15 - Switching Time Test Circuit

Fig. 16 - Gate Charge Test Circuit

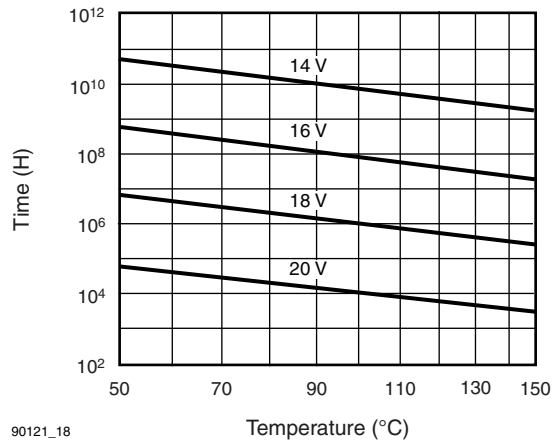


Fig. 17 - Typical Time to Accumulated 1 % Gate Failure

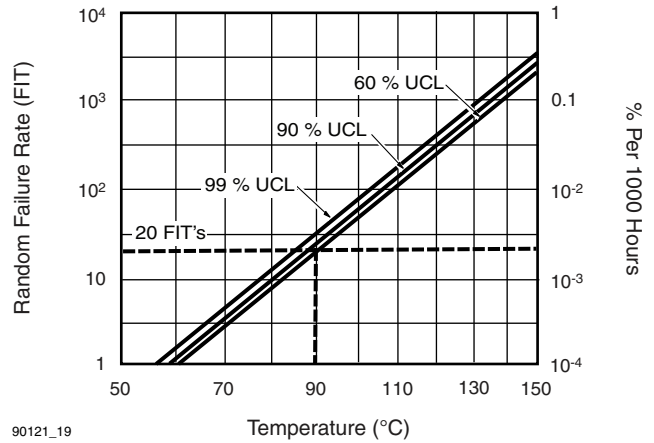


Fig. 18 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

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