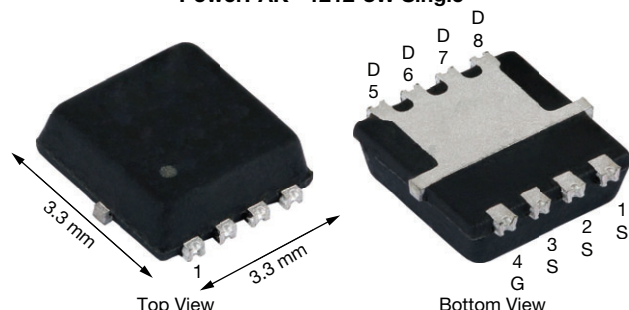


Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8W Single

Marking code: Q034

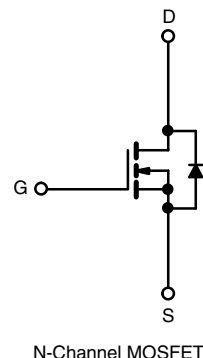
PRODUCT SUMMARY

V_{DS} (V)	30
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.0085
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0100
I_D (A)	16
Configuration	Single
Package	PowerPAK 1212-8W

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified ^d
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ^a	I_D	$T_C = 25$ °C	16
		$T_C = 125$ °C	16
Continuous source current (diode conduction) ^a	I_S	16	A
Pulsed drain current ^b	I_{DM}	64	
Single pulse avalanche current	I_{AS}	31	
Single pulse avalanche energy	E_{AS}	48	mJ
Maximum power dissipation ^b	P_D	$T_C = 25$ °C	62
		$T_C = 125$ °C	20
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{e, f}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	81	°C/W
Junction-to-case (drain)	R_{thJC}	2.4	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- Parametric verification ongoing
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 30 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 175 °C	-	-	150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	20	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 16.4 A	-	0.0070	0.0085	Ω
		V _{GS} = 10 V	I _D = 16.4 A, T _J = 125 °C	-	-	0.0135	
		V _{GS} = 10 V	I _D = 16.4 A, T _J = 175 °C	-	-	0.0160	
		V _{GS} = 4.5 V	I _D = 16.4 A	-	0.0080	0.0100	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 16.4 A		-	70	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	1492	1865	pF
Output capacitance	C _{oss}			-	280	350	
Reverse transfer capacitance	C _{rss}			-	108	135	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 15 V, I _D = 10 A	-	26	39	nC
Gate-source charge ^c	Q _{gs}			-	4.7	-	
Gate-drain charge ^c	Q _{gd}			-	4.3	-	
Gate resistance	R _g	f = 1 MHz		5	10	20	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		-	7	11	ns
Rise time ^c	t _r			-	21	32	
Turn-off delay time ^c	t _{d(off)}			-	49	74	
Fall Time ^c	t _f			-	18	27	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	64	A
Forward voltage	V _{SD}	I _F = 15 A, V _{GS} = 0		-	0.82	1.2	V

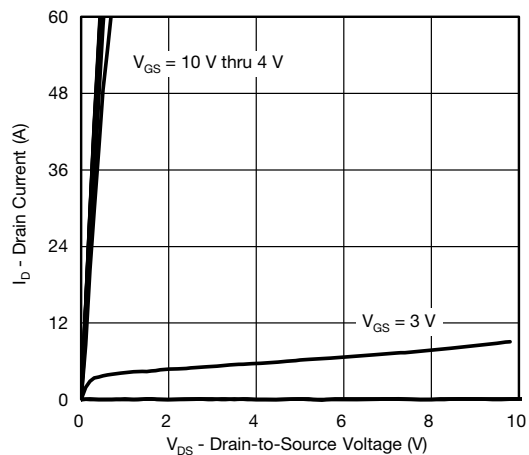
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

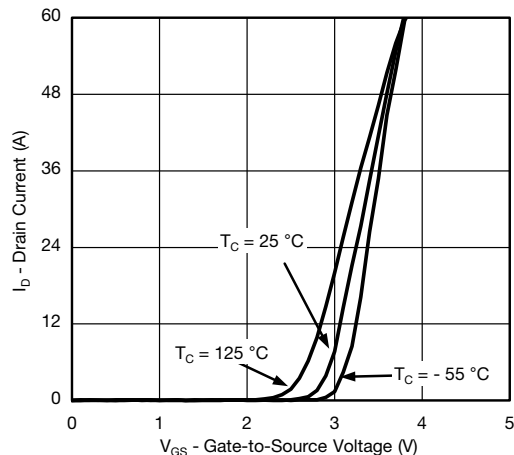
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



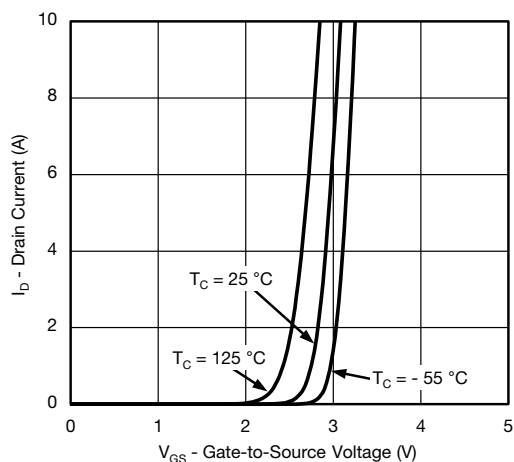
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



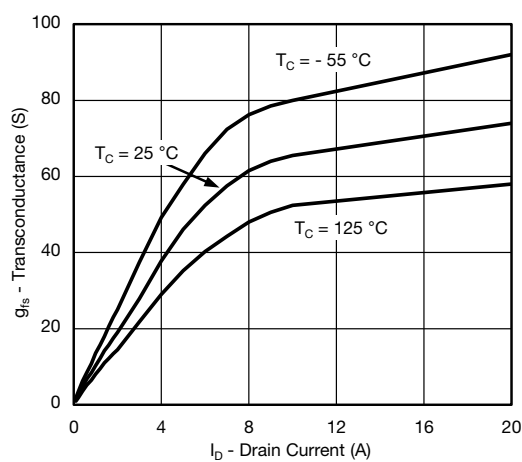
Output Characteristics



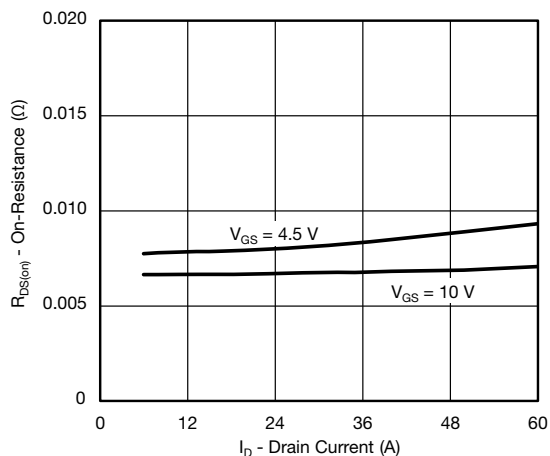
Transfer Characteristics



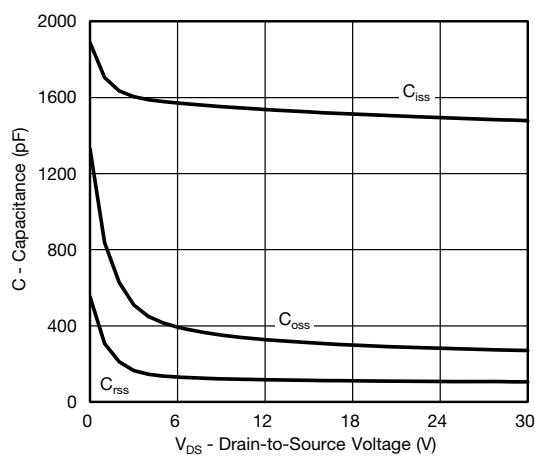
Transfer Characteristics



Transconductance



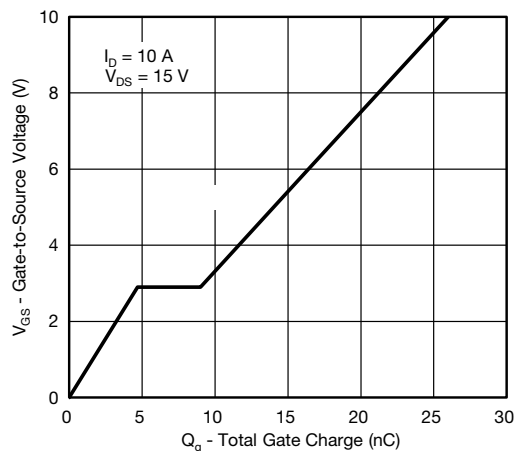
On-Resistance vs. Drain Current



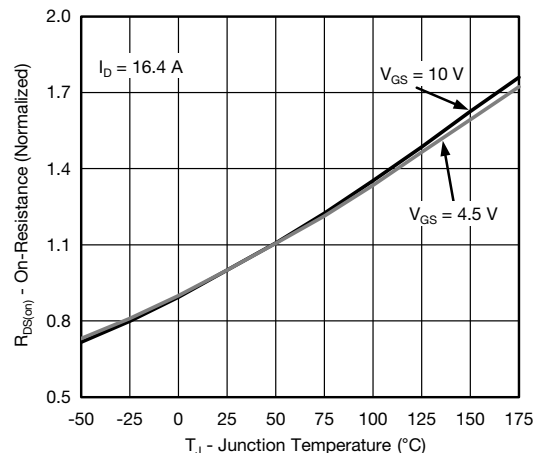
Capacitance



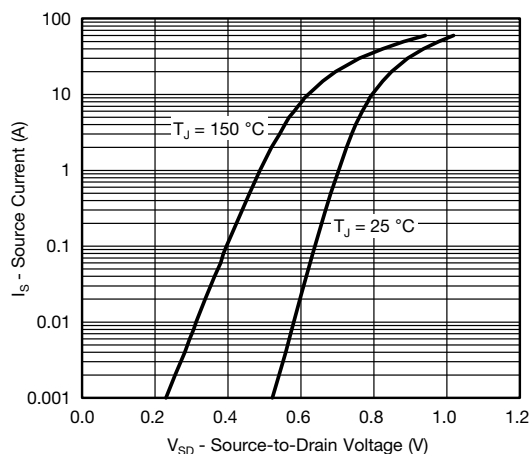
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



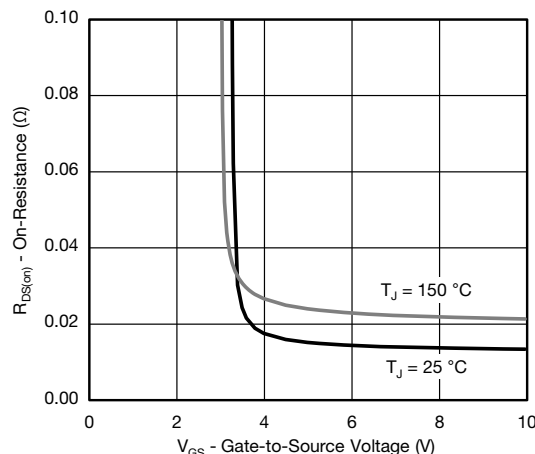
Gate Charge



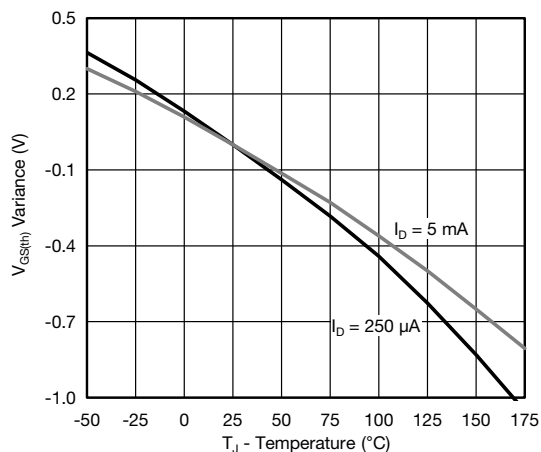
On-Resistance vs. Junction Temperature



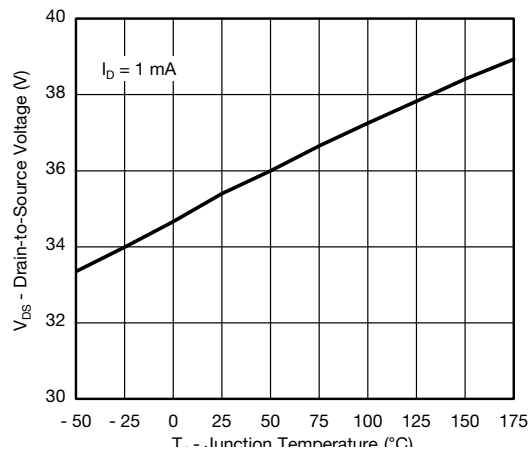
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



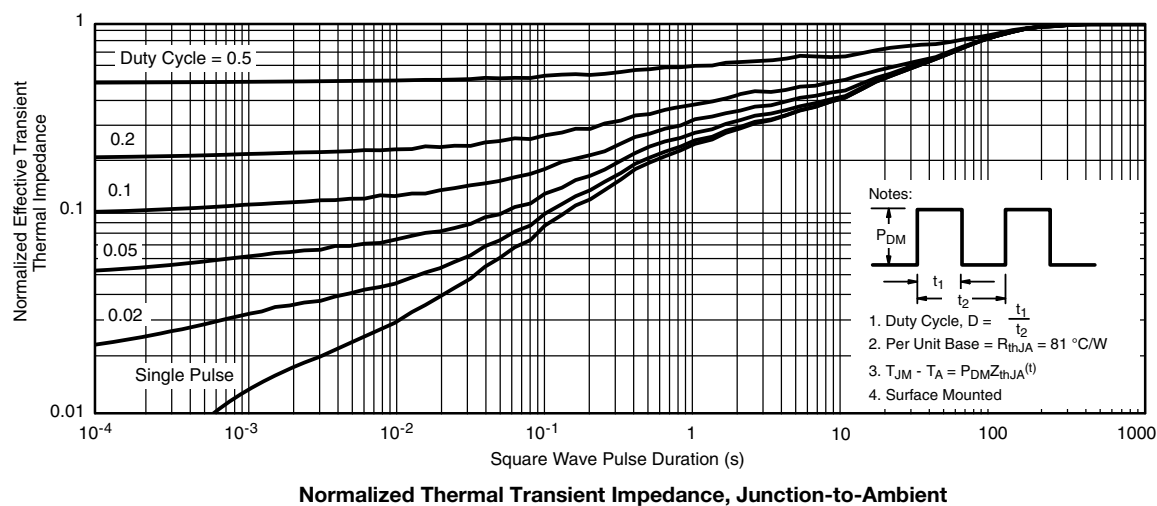
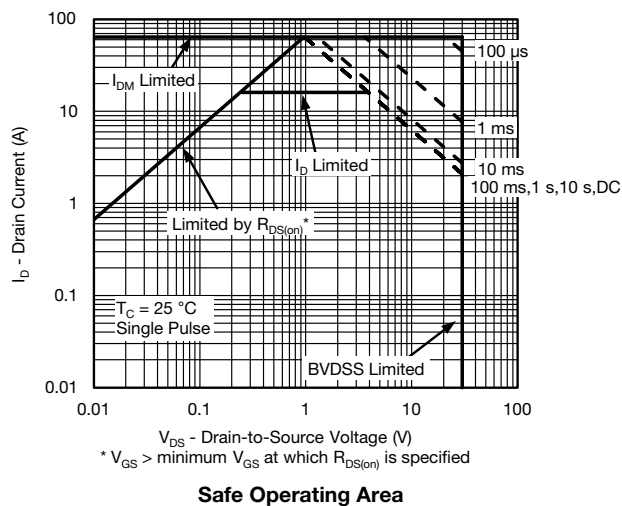
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

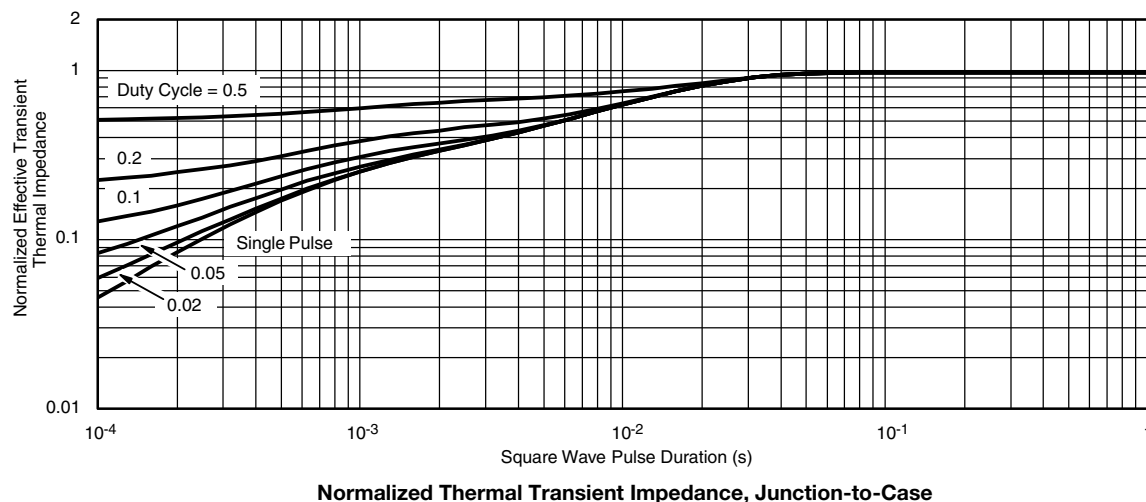


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)





THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

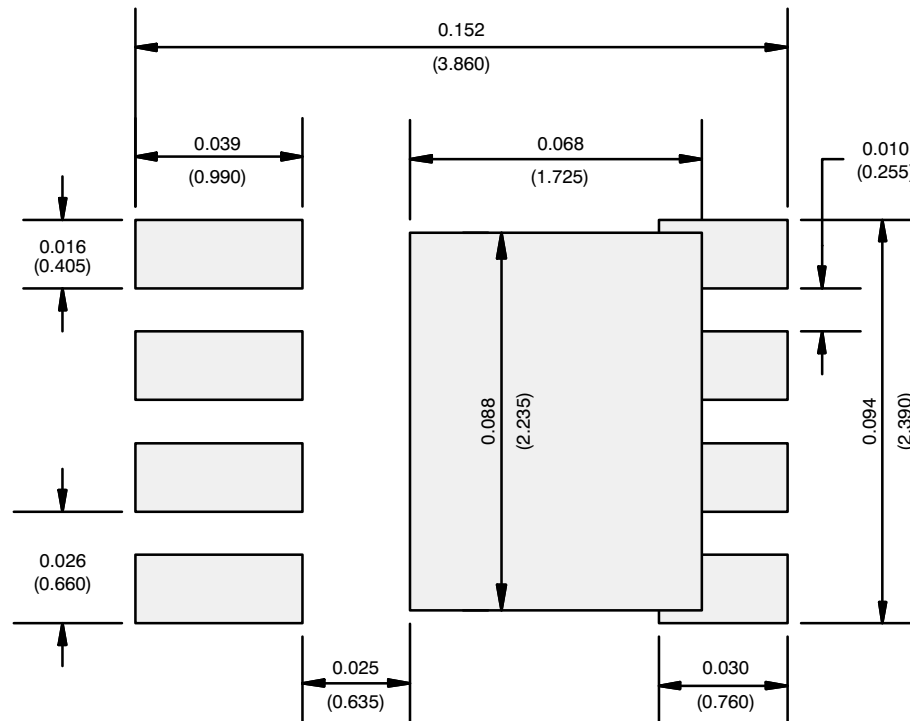


Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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