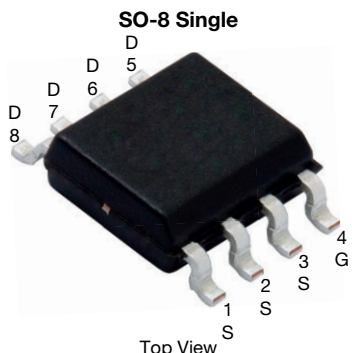


N-Channel 30 V (D-S) MOSFET



FEATURES

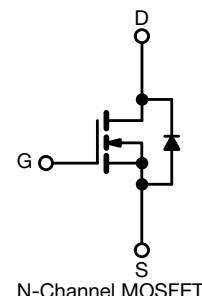
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Low side DC/DC conversion
 - Notebook
 - Gaming



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00275
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00340
Q_g typ. (nC)	30
I_D (A) ^a	39
Configuration	Single

ORDERING INFORMATION	
Package	SO-8
Lead (Pb)-free and halogen-free	Si4126DY-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	39	A
	$T_C = 70^\circ\text{C}$		31	
	$T_A = 25^\circ\text{C}$		26.5 ^{b, c}	
	$T_A = 70^\circ\text{C}$		21 ^{b, c}	
Pulsed drain current		I_{DM}	70	
Continuous source-drain diode current	$T_C = 25^\circ\text{C}$	I_S	7	
	$T_A = 25^\circ\text{C}$		3.1 ^{b, c}	
Single pulse avalanche current		I_{AS}	40	
Avalanche energy		E_{AS}	80	mJ
Maximum power dissipation	$T_C = 25^\circ\text{C}$	P_D	7.8	W
	$T_C = 70^\circ\text{C}$		5	
	$T_A = 25^\circ\text{C}$		3.5 ^{b, c}	
	$T_A = 70^\circ\text{C}$		2.2 ^{b, c}	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	t ≤ 10 s	R _{thJA}	29	35	°C/W
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	13	16	

Notes

- Based on $T_C = 25^\circ\text{C}$
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- Maximum under steady state conditions is 80°C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	24	-	mV/°C	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-6.4	-		
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.5	V	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10		
On-state drain current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30	-	-	A	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	-	0.00220	0.00275	Ω	
		V _{GS} = 4.5 V, I _D = 10 A	-	0.00270	0.00340		
Forward transconductance ^a	g _{fs}	V _{GS} = 15 V, I _D = 15 A	-	75	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	4405	-	pF	
Output capacitance	C _{oss}		-	760	-		
Reverse transfer capacitance	C _{rss}		-	285	-		
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	-	70	105	nC	
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	-	30	45		
Q _{gs}	-		10.2	-			
Q _{gd}	-		7.4	-			
Gate resistance	R _g	f = 1 MHz	0.3	1.4	2.8	Ω	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	36	60	ns	
Rise time	t _r		-	20	40		
Turn-off delay time	t _{d(off)}		-	53	90		
Fall time	t _f		-	24	40		
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	15	30		
Rise time	t _r		-	10	20		
Turn-off delay time	t _{d(off)}		-	43	70		
Fall time	t _f		-	10	20		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	7	A	
Pulse diode forward current ^a	I _{SM}		-	-	70		
Body diode voltage	V _{SD}	I _S = 3 A	-	0.71	1.1	V	
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	38	60	ns	
Body diode reverse recovery charge	Q _{rr}		-	38	60	nC	
Reverse recovery fall time	t _a		-	19	-	ns	
Reverse recovery rise time	t _b		-	20	-		

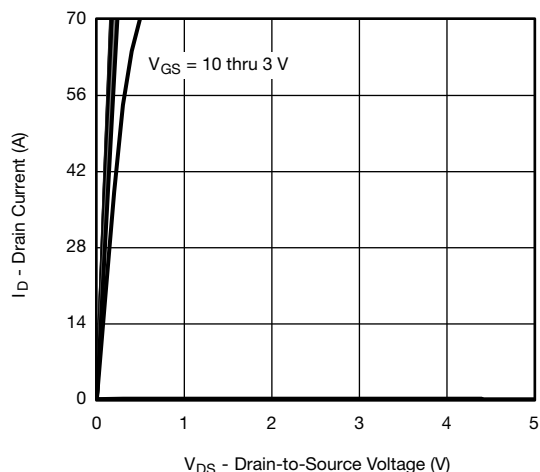
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

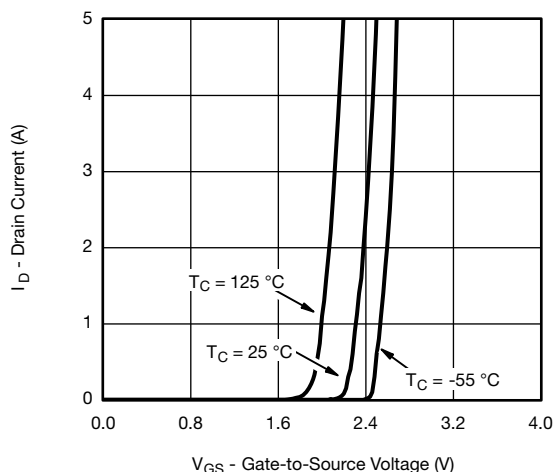
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



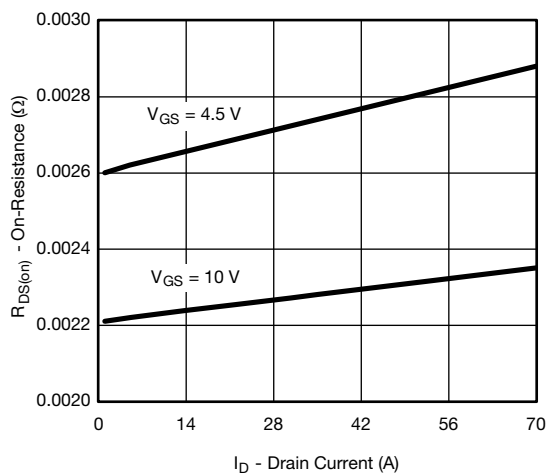
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



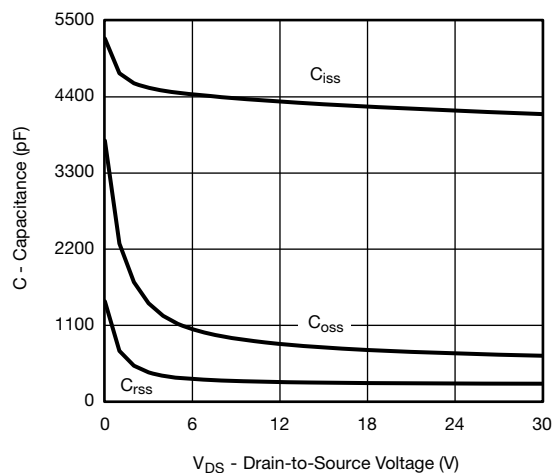
Output Characteristics



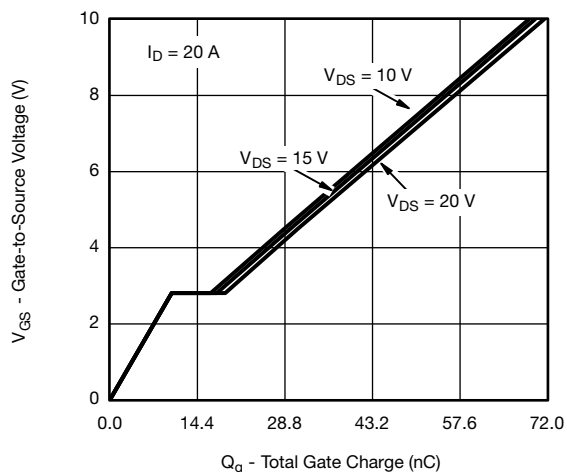
Transfer Characteristics



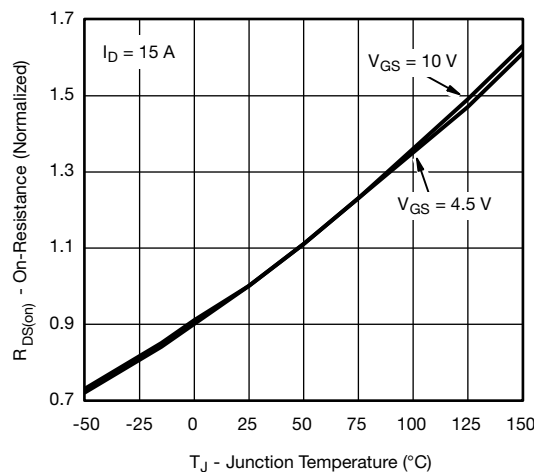
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



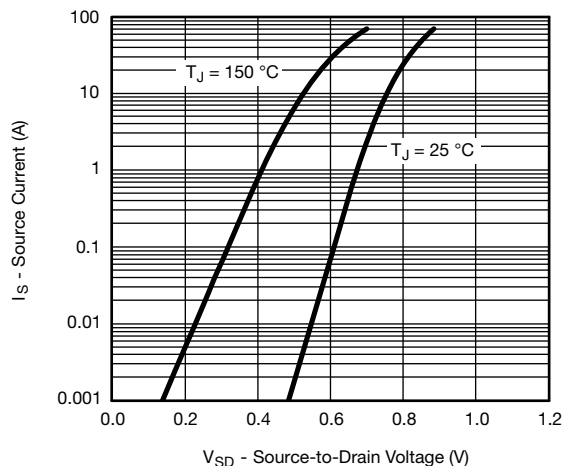
Gate Charge



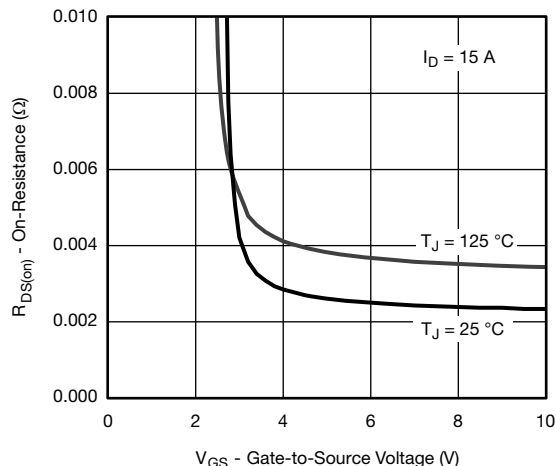
On-Resistance vs. Junction Temperature



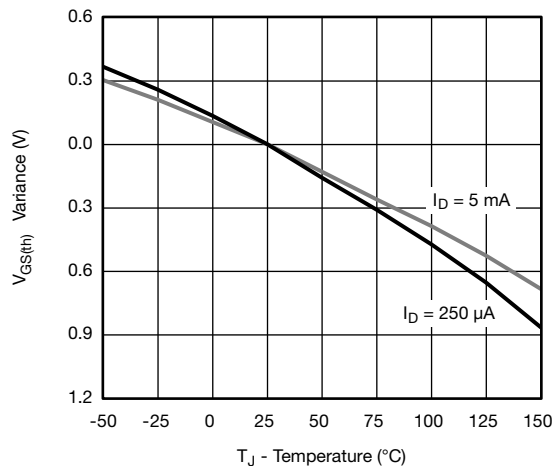
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



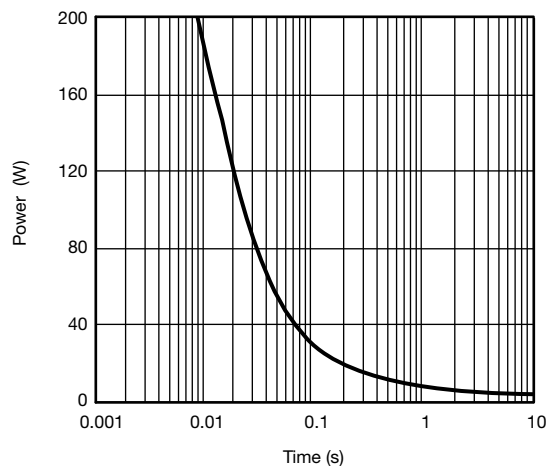
Source-Drain Diode Forward Voltage



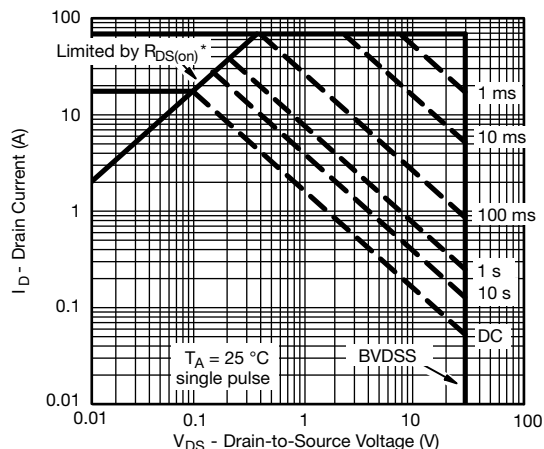
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



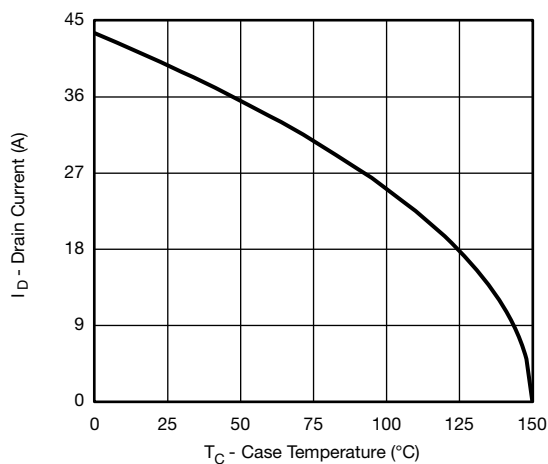
Single Pulse Power, Junction-to-Ambient



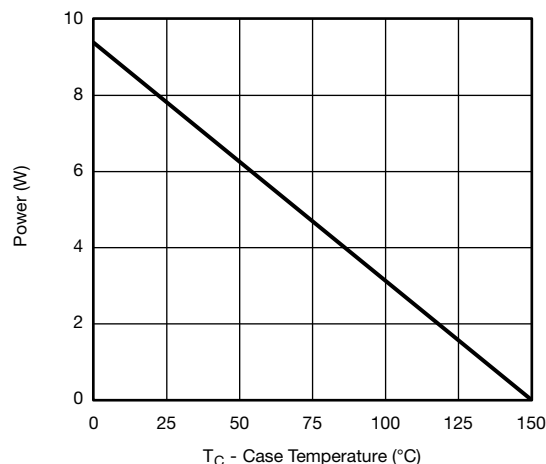
Safe Operating Area, Junction-to-Ambient



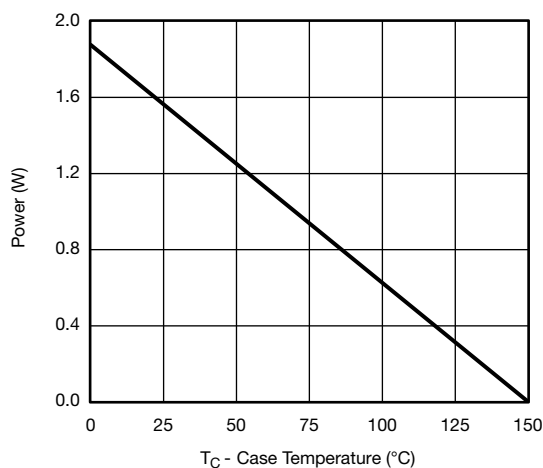
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Case



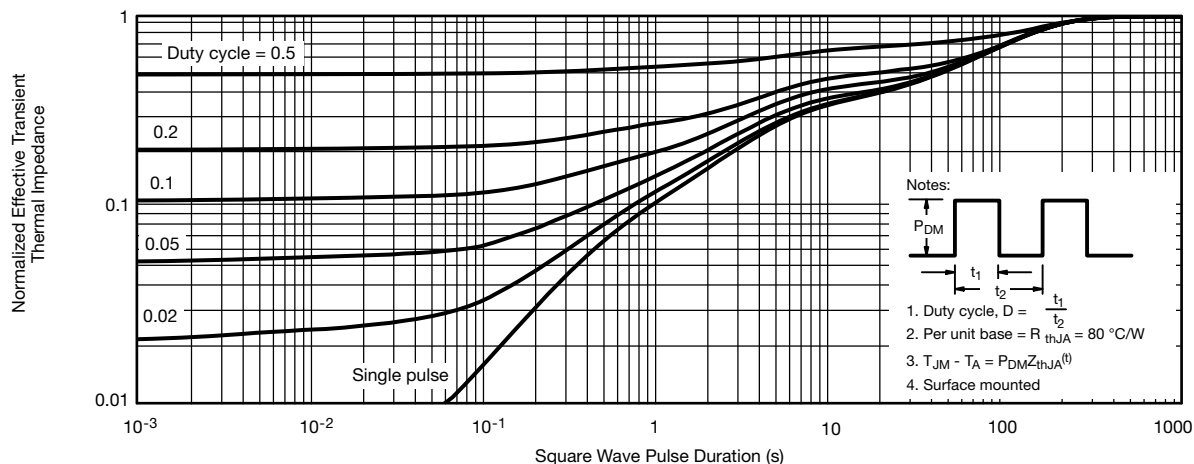
Power, Junction-to-Ambient

Note

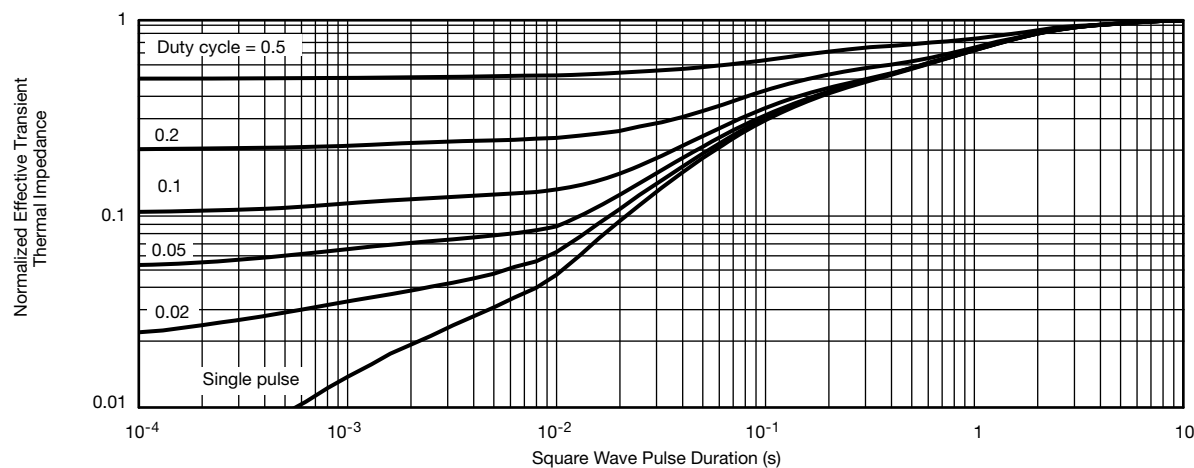
- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

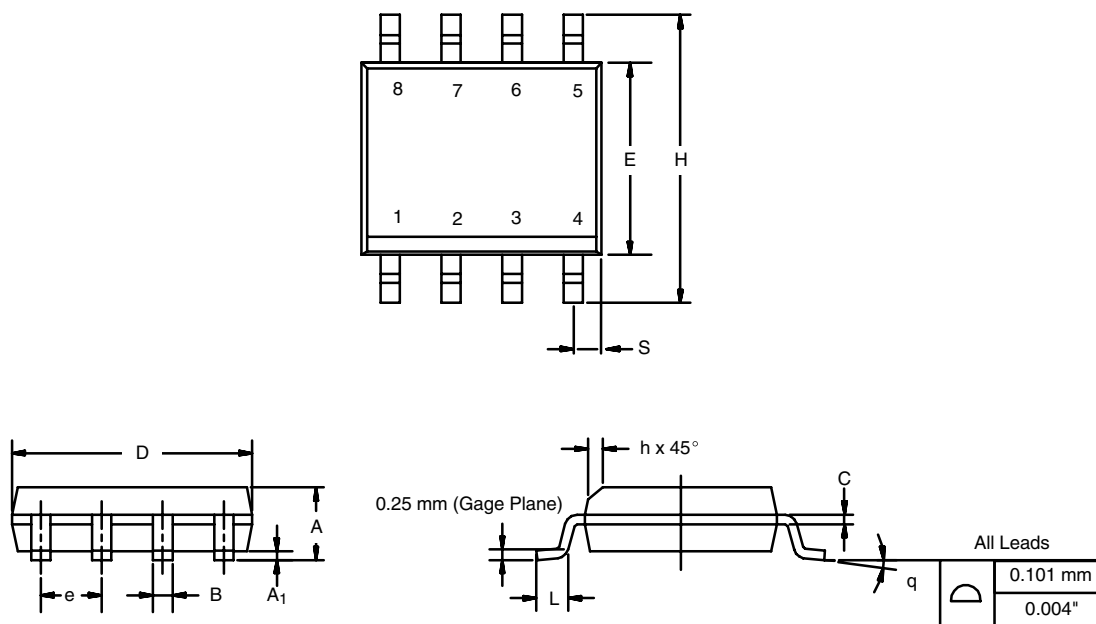


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69994.

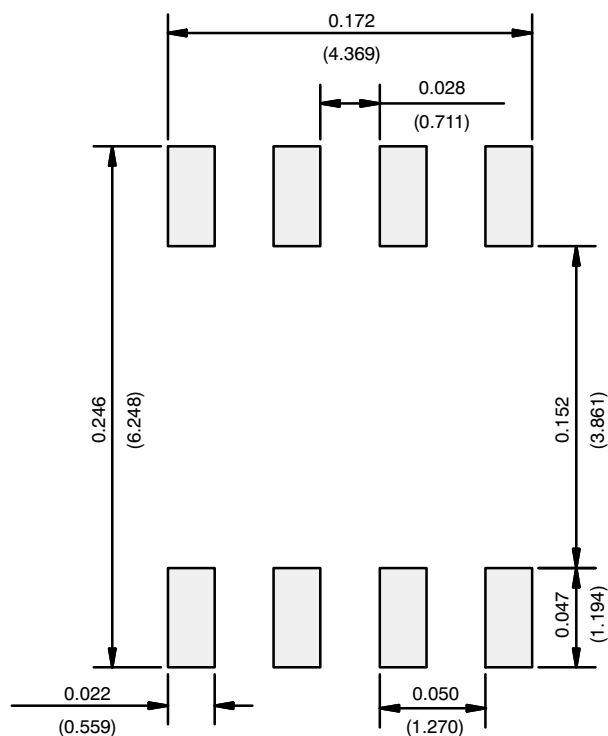
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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