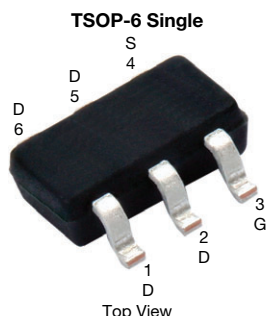


N-Channel 20 V (D-S) MOSFET



Marking code: AZ

PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.024
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 2.5$ V	0.028
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 1.8$ V	0.030
Q_g typ. (nC)	11
I_D (A) ^{a, e}	8
Configuration	Single

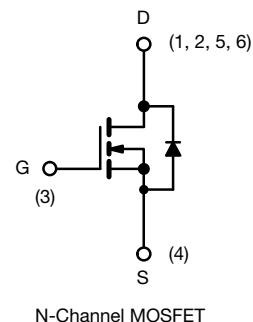
FEATURES

- TrenchFET[®] power MOSFET
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- DC/DC converters
- Load switch for portable applications



ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free and halogen-free	Si3464DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	20	V	
Gate-source voltage	V_{GS}	± 8		
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	8 ^a	A	
	$T_C = 70$ °C	8 ^a		
	$T_A = 25$ °C	7.5 ^{b, c}		
	$T_A = 70$ °C	6 ^{b, c}		
Pulsed drain current	I_{DM}	20		
Continuous source-drain diode current	$T_C = 25$ °C	3		
	$T_A = 25$ °C	1.7 ^{b, c}		
Maximum power dissipation	$T_C = 25$ °C	3.6	W	
	$T_C = 70$ °C	2.3		
	$T_A = 25$ °C	2 ^{b, c}		
	$T_A = 70$ °C	1.3 ^{b, c}		
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature)		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	$t \leq 5$ s	50	62.5	°C/W
Maximum junction-to-foot (drain)	Steady state	28	35	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 110 °C/W
- Based on $T_C = 25$ °C



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20	-	-	V	
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 250 μA	-	23	-	mV/°C	
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	-2.6	-		
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.45	-	1	V	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	-	-	1	μA	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	10		
On-state drain current ^a	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = 4.5 V	20	-	-	A	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 7.5 A	-	0.020	0.024	Ω	
		V _{GS} = 2.5 V, I _D = 7 A	-	0.023	0.028		
		V _{GS} = 1.8 V, I _D = 6.7 A	-	0.025	0.030		
Forward transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 7.5 A	-	17	-	S	
Dynamic ^b							
Input capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	-	1065	-	pF	
Output capacitance	C _{oss}		-	150	-		
Reverse transfer capacitance	C _{rss}		-	70	-		
Total gate charge	Q _g	V _{DS} = 10 V, V _{GS} = 5 V, I _D = 7.5 A	-	12	18	nC	
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 7.5 A	-	11	17		
Q _{gs}	-		1.8	-			
Q _{gd}	-		1.1	-			
Gate resistance	R _g	f = 1 MHz	0.4	2.2	4.4	Ω	
Turn-on delay time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.7 Ω I _D ≅ 6 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	5	10	ns	
Rise time	t _r		-	15	23		
Turn-off delay time	t _{d(off)}		-	43	65		
Fall time	t _f		-	10	20		
Turn-on delay time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.7 Ω I _D ≅ 6 A, V _{GEN} = 5 V, R _g = 1 Ω	-	3	6		
Rise time	t _r		-	12	18		
Turn-off delay time	t _{d(off)}		-	22	33		
Fall time	t _f		-	8	16		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	3	A	
Pulse diode forward current	I _{SM}		-	-	20		
Body diode voltage	V _{SD}	I _S = 6 A, V _{GS} = 0 V	-	0.75	1.2	V	
Body diode reverse recovery time	t _{rr}	I _F = 6 A, di/dt = 100 A/μs, T _J = 25 °C	-	15	23	ns	
Body diode reverse recovery charge	Q _{rr}		-	6	12	nC	
Reverse recovery fall time	t _a		-	8	-	ns	
Reverse recovery rise time	t _b		-	7	-		

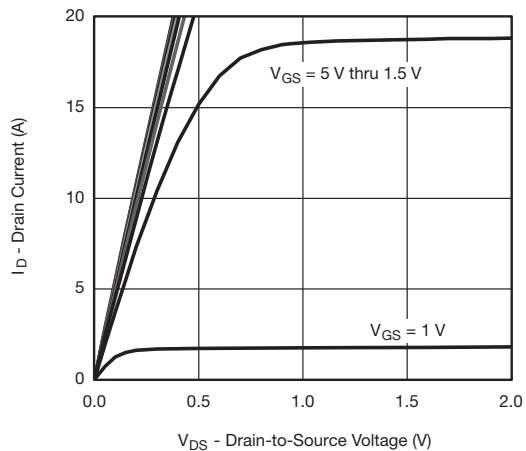
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

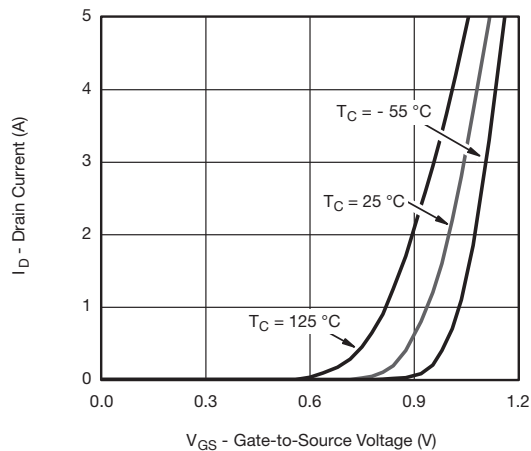
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



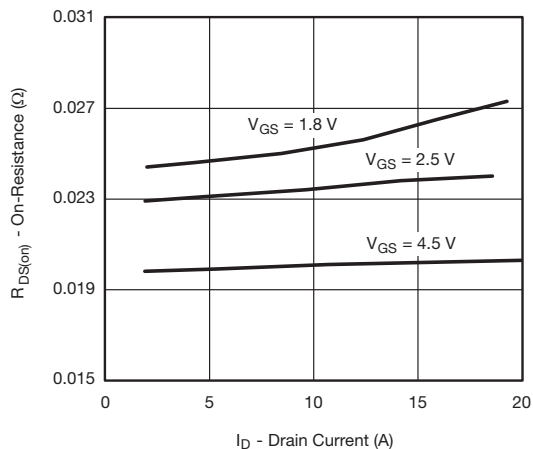
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



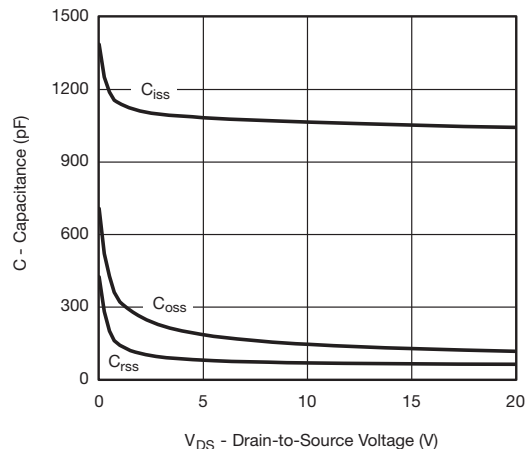
Output Characteristics



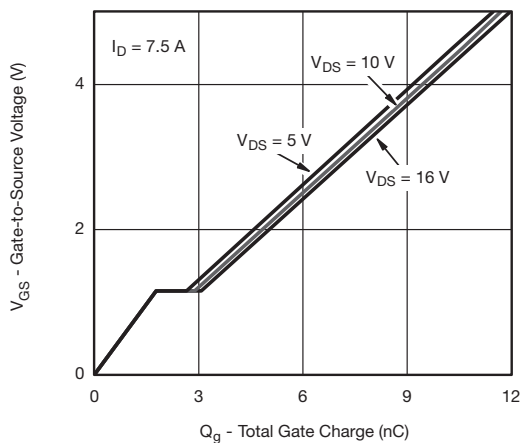
Transfer Characteristics



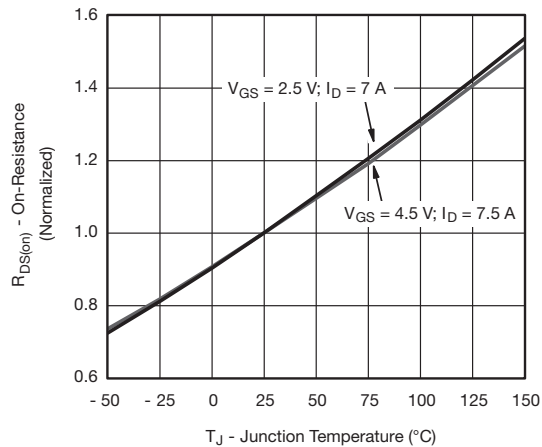
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



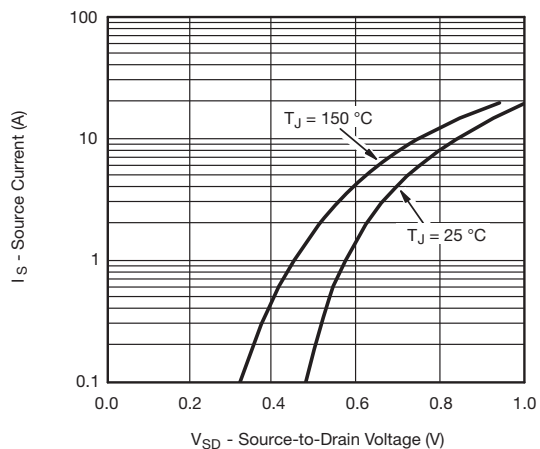
Gate Charge



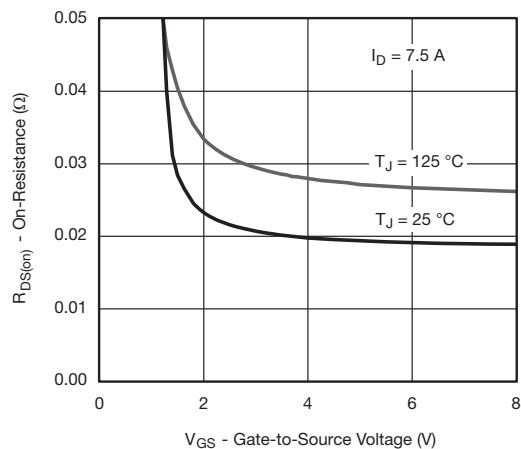
On-Resistance vs. Junction Temperature



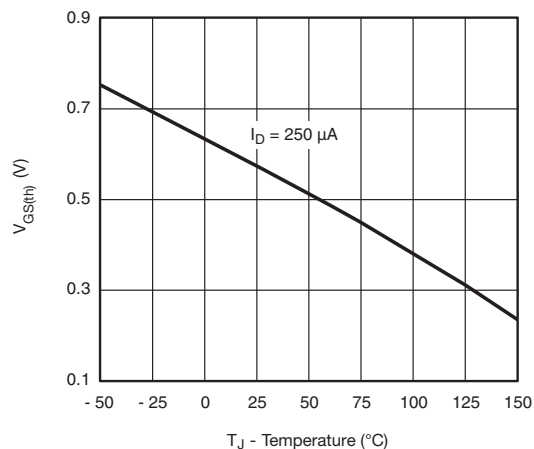
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



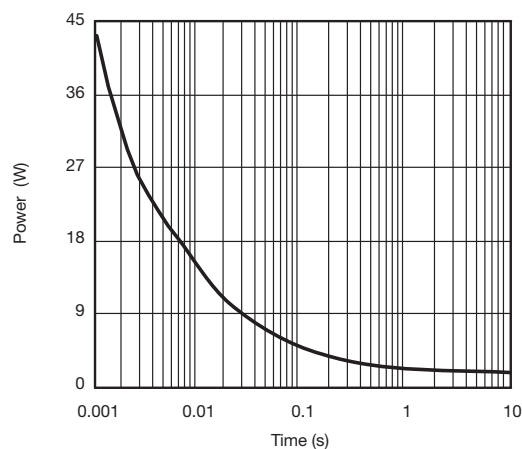
Source-Drain Diode Forward Voltage



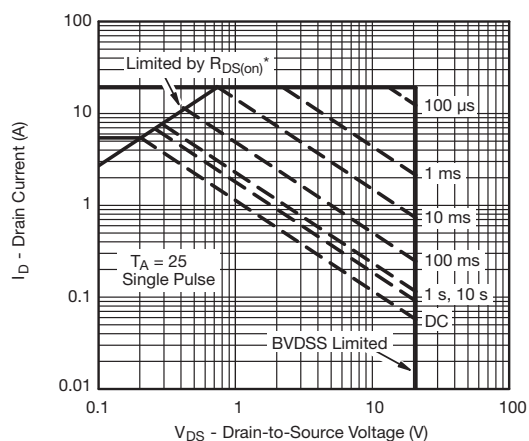
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



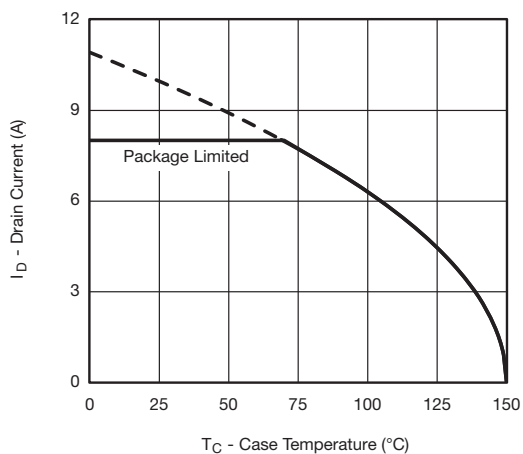
Single Pulse Power (Junction-to-Ambient)



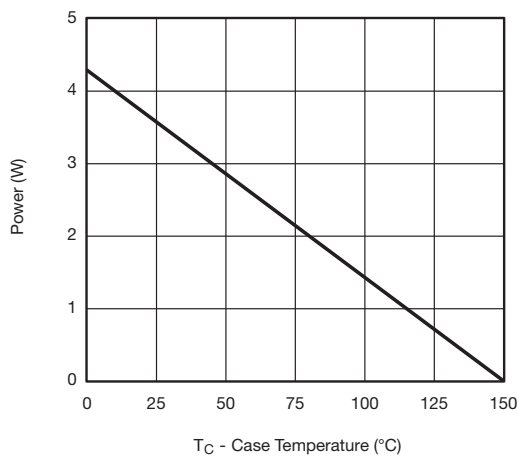
Safe Operating Area, Junction-to-Ambient



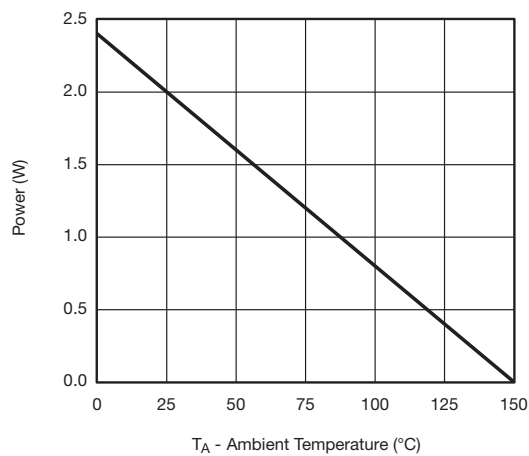
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power Derating, Junction-to-Foot



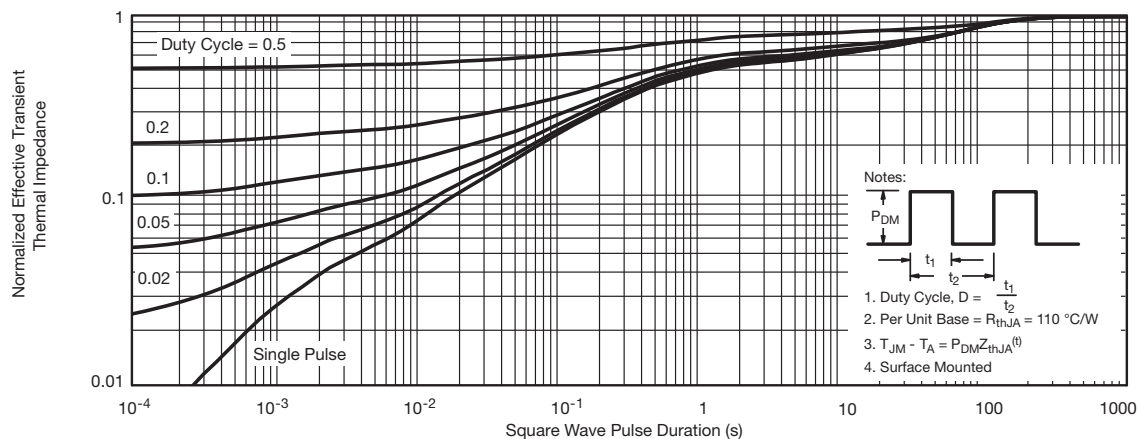
Power Derating, Junction-to-Ambient

Note

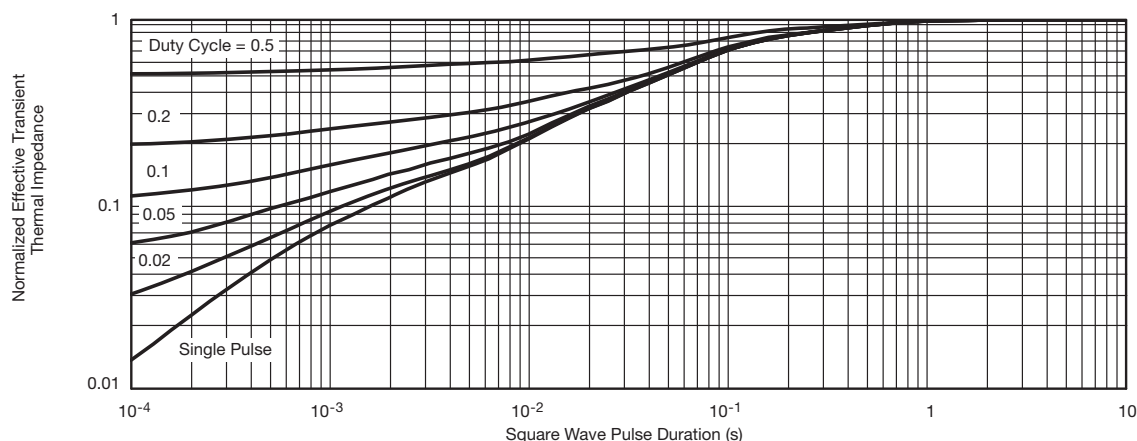
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65712.

TSOP: 5/6-LEAD

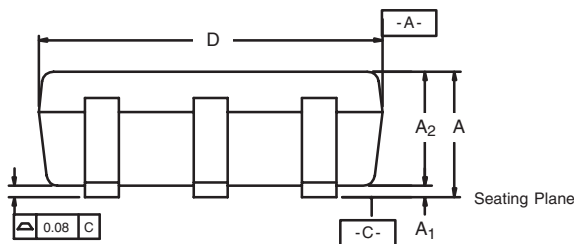
JEDEC Part Number: MO-193C



5-LEAD TSOP

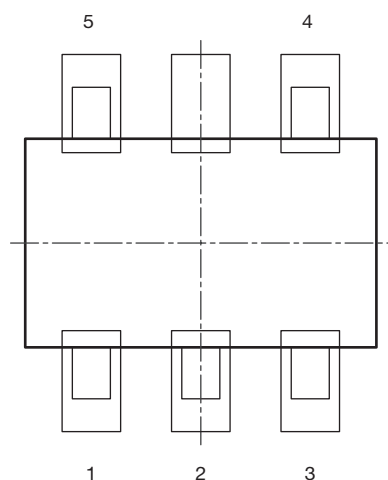


6-LEAD TSOP

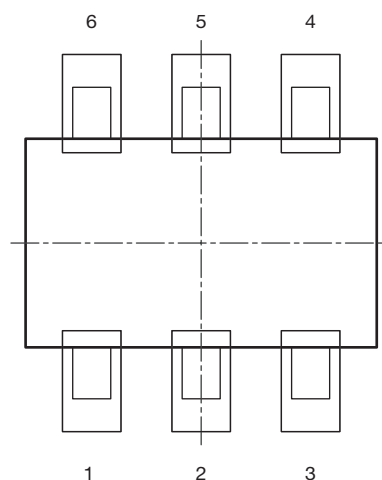


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

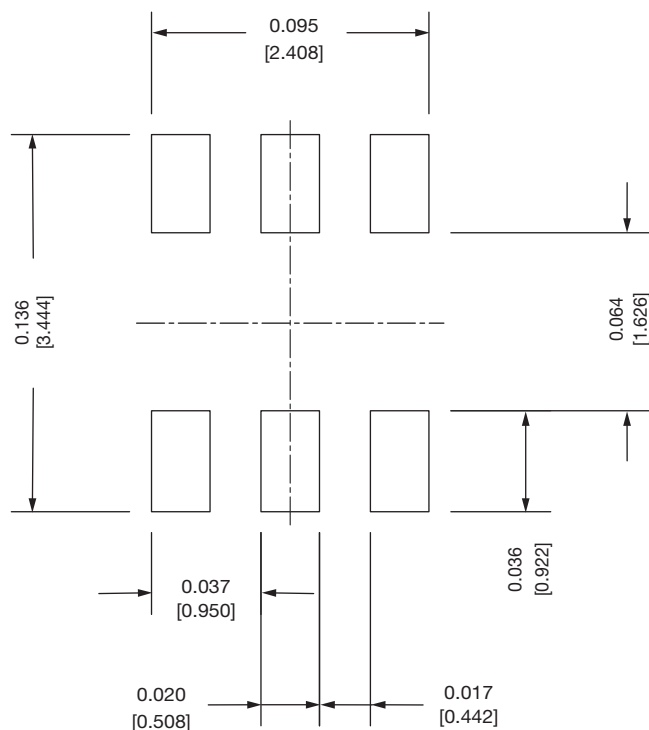
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L



Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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