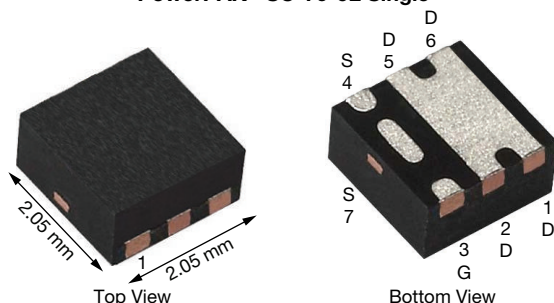


P-Channel 20 V (D-S) MOSFET

PowerPAK® SC-70-6L Single


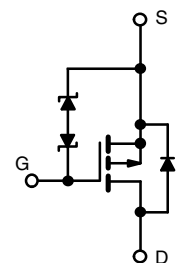
FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Thermally enhanced PowerPAK® SC-70 package
 - Small footprint area
 - Low on-resistance
- Typical ESD protection: 3000 V (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power management for portable and consumer
 - Load switches
 - Battery switches
 - Charger switches



P-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	-20
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0320
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -2.5$ V	0.0410
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -1.8$ V	0.0675
Q_g typ. (nC)	13.8
I_D (A) ^{a, e}	-9
Configuration	Single

Marking Code: KC

ORDERING INFORMATION

Package	PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA4265EDJ-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-20	V
Gate-source voltage	V_{GS}	± 8	
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	-9 ^e
		$T_C = 70$ °C	-9 ^e
		$T_A = 25$ °C	-7.8 ^{b, c}
		$T_A = 70$ °C	-6.2 ^{b, c}
Pulsed drain current ($t = 300$ μ s)	I_{DM}	-20	
Continuous source-drain diode current	I_S	$T_C = 25$ °C	-9 ^e
		$T_A = 25$ °C	-2.4
Maximum power dissipation	P_D	$T_C = 25$ °C	15.6
		$T_C = 70$ °C	10
		$T_A = 25$ °C	2.9 ^{b, c}
		$T_A = 70$ °C	1.8 ^{b, c}
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, d}	R_{thJA}	32	43	°C/W
Maximum junction-to-foot (drain)	R_{thJF}	6	8	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 5$ s
- Maximum under steady state conditions is 80 °C/W
- Package limited

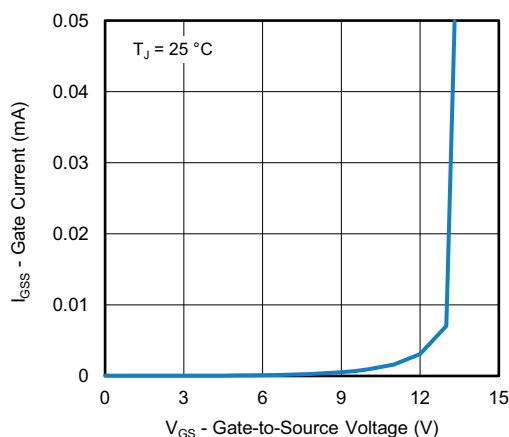
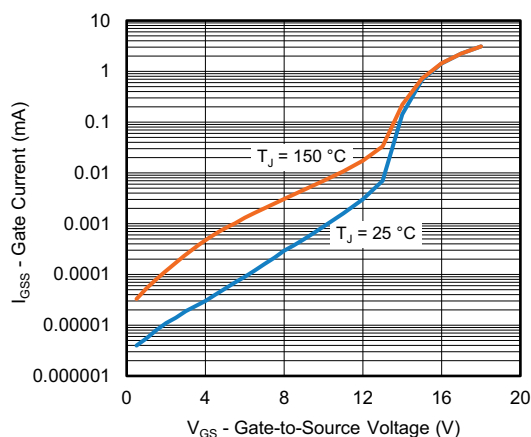
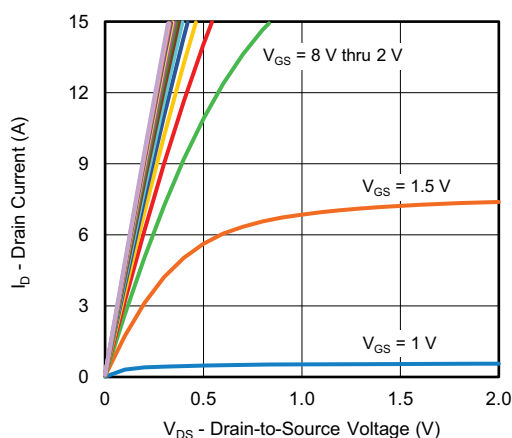
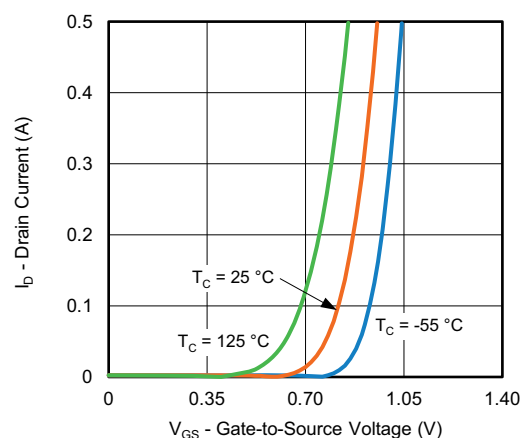
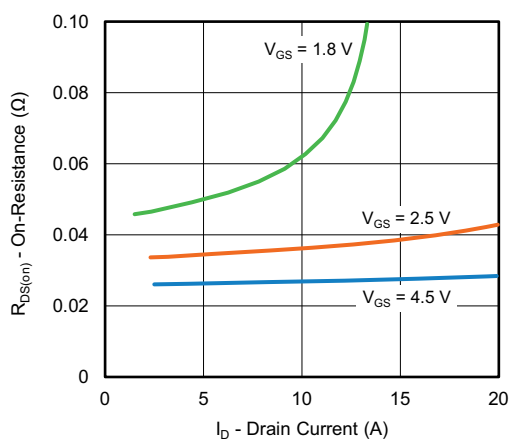
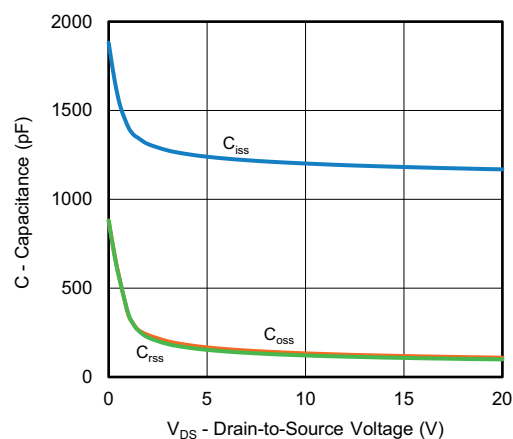


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-20	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -250 μA	-	-14	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J		-	2.5	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.4	-	-1	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	-	-	± 10	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V	-	-	± 1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -4 A	-	0.0265	0.0320	Ω
		V _{GS} = -2.5 V, I _D = -4 A	-	0.0340	0.0410	
		V _{GS} = -1.8 V, I _D = -2 A	-	0.0465	0.0675	
Dynamic ^b						
Input capacitance	C _{iss}	V _S = 0 V, f = 1 MHz	-	1180	-	pF
Output capacitance	C _{oss}		-	135	-	
Reverse transfer capacitance	C _{rss}		-	130	-	
Total gate charge	Q _g	V _{DS} = -10 V, V _{GS} = -8 V, I _D = -4.5 A	-	23.8	36	nC
		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -4.5 A	-	13.8	21	
Q _{gs}	-		1.9	-		
Gate-source charge	Q _{gd}		-	3	-	
Gate-drain charge	Q _{gd}					
Gate resistance	R _g	f = 1 MHz	2.2	11	22	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.8 Ω I _D ≡ -3.6 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	22	33	ns
Rise time	t _r		-	21	32	
Turn-off delay time	t _{d(off)}		-	62	93	
Fall time	t _f		-	14	21	
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 2.8 Ω I _D ≡ -3.6 A, V _{GEN} = -8 V, R _g = 1 Ω	-	9	18	
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	65	98	
Fall time	t _f		-	15	23	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-1.4	A
Pulse diode forward current	I _{SM}		-	-	-20	
Body diode voltage	V _{SD}	I _S = -3.6 A, V _{GS} = 0 V	-	-0.8	-1.2	V
Body diode reverse recovery time	t _{rr}	I _F = -3.6 A, di/dt = 100 A/μs, T _J = 25 °C	-	13	20	ns
Body diode reverse recovery charge	Q _{rr}		-	5	10	nC
Reverse recovery fall time	t _a		-	8	-	ns
Reverse recovery rise time	t _b		-	5	-	

Notes

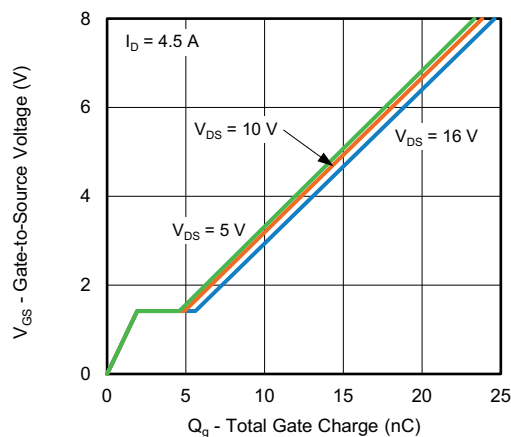
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

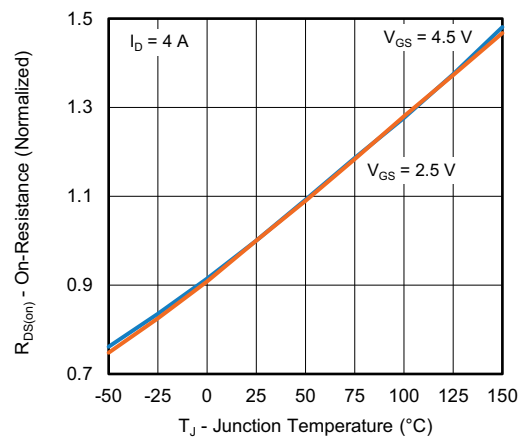
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance



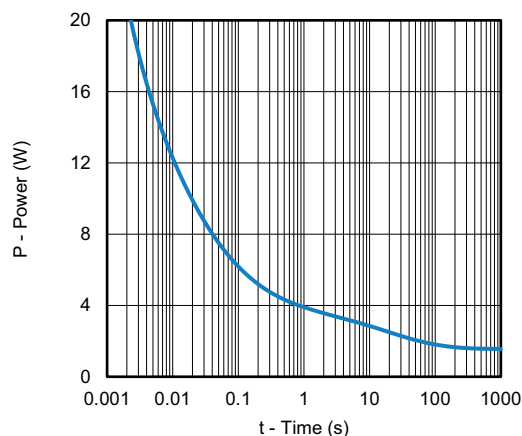
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



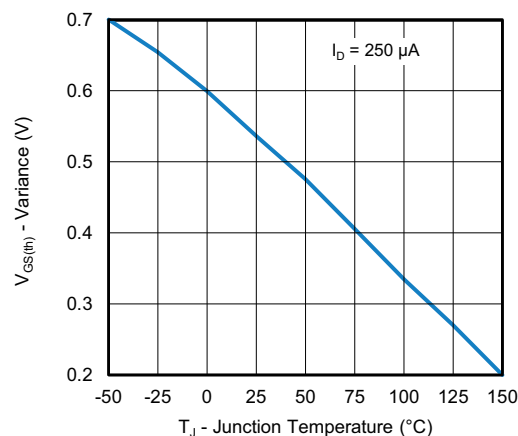
Gate Charge



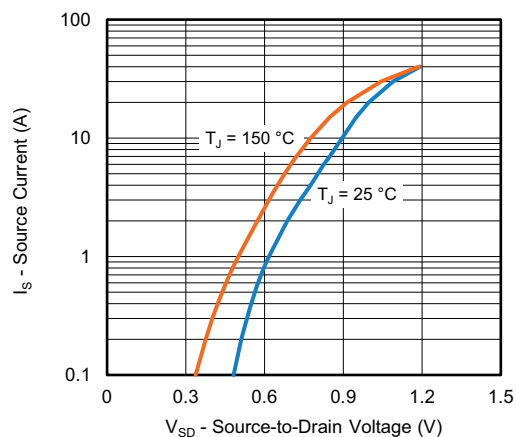
On-Resistance vs. Junction Temperature



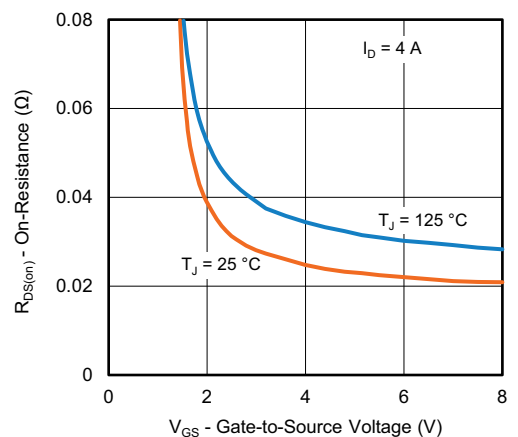
Single Pulse Power, Junction-to-Ambient



Threshold Voltage



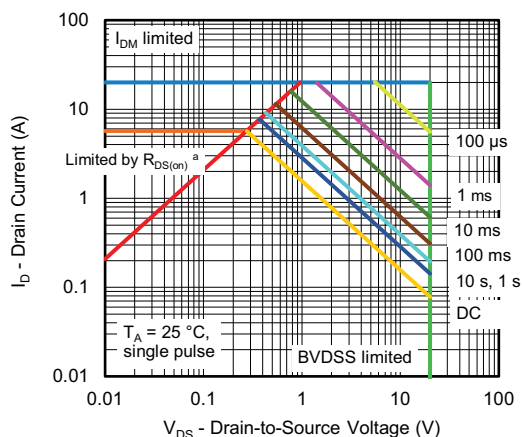
Source-Drain Diode Forward Voltage



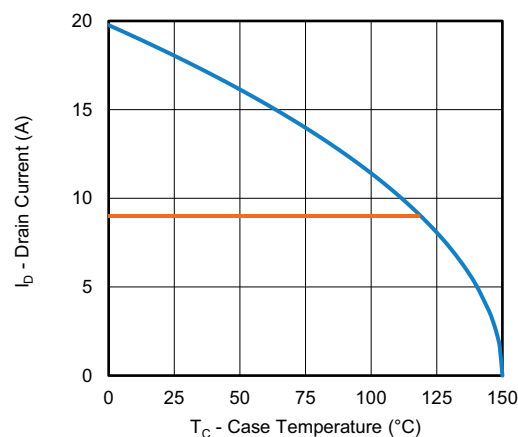
On-Resistance vs. Gate-to-Source Voltage



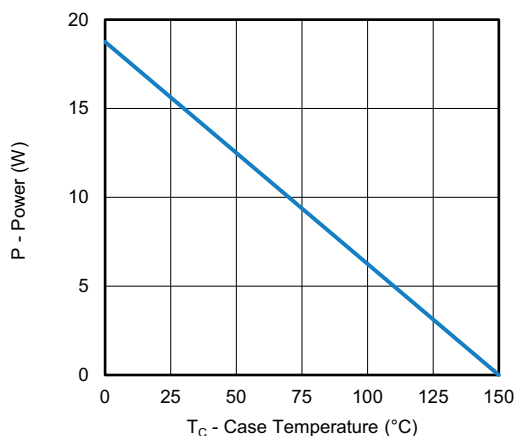
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



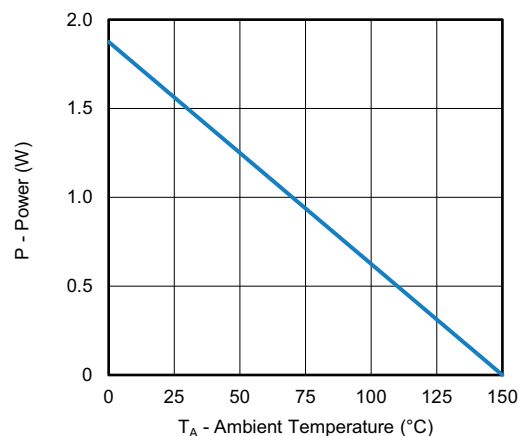
Safe Operating Area, Junction-to-Ambient



Current Derating ^a



Power Junction-to-Case



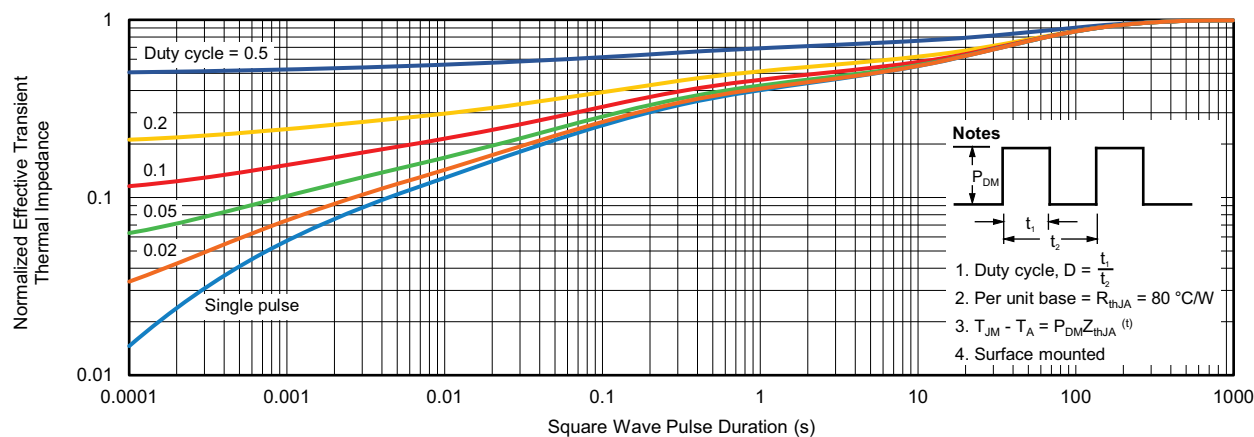
Power Junction-to-Ambient

Note

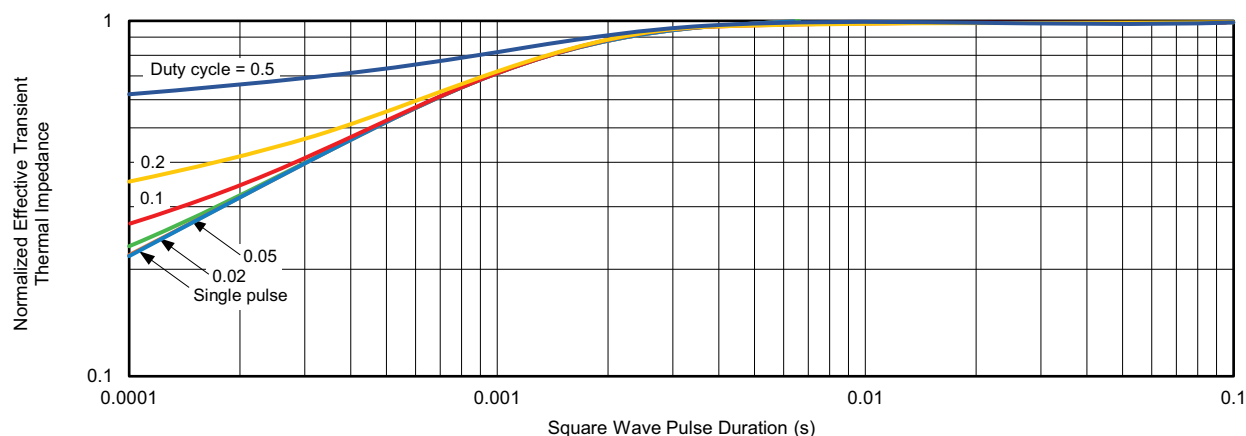
- a. The power dissipation P_D is based on T_J max. = 150 $^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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