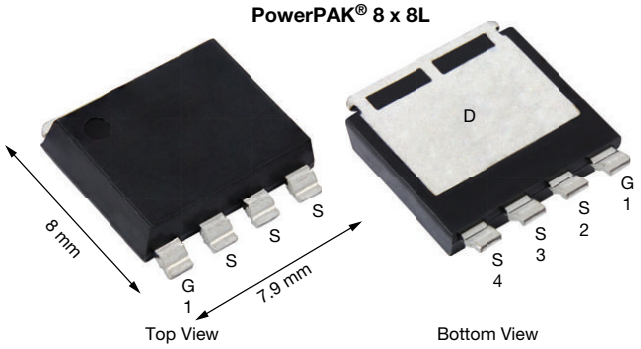
Automotive P-Channel 80 V (D-S) 175 °C MOSFET



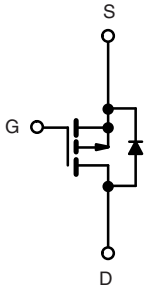
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

RoHS COMPLIANT

HALOGEN FREE



P-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	-80
$R_{DS(on)}$ (Ω) at V_{GS} = -10 V	0.0055
$R_{DS(on)}$ (Ω) at V_{GS} = -4.5 V	0.0077
I_D (A) [g]	-175
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and Halogen-free	SQJQ181EL

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-80	V
Gate-source voltage [a]		V_{GS}	± 20	
Continuous drain current [g]	T_C = 25 °C [b]	I_D	-175	A
	T_C = 125 °C		-101	
Continuous source current (diode conduction) [b, g]		I_S	-317	
Pulsed drain current [c, g]		I_{DM}	-619	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-78	
Single pulse avalanche energy		E_{AS}	305	mJ
Maximum power dissipation [c, g]	T_C = 25 °C	P_D	348	W
	T_C = 125 °C		116	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [e]	R_{thJA}	42	°C/W
Junction-to-case (drain) [f]		R_{thJC}	0.43	

Notes

a. Not intended for continuous use with positive gate voltage > 5.0 V
b. Package limited
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). For PowerPAK SO-8L, the end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
f. Using thermal characterization methods based on JESD51-14
g. Values based on R_{thJC} and T_C of 25 °C. Actual values achievable will be dependent on the thermal characteristics of the complete system

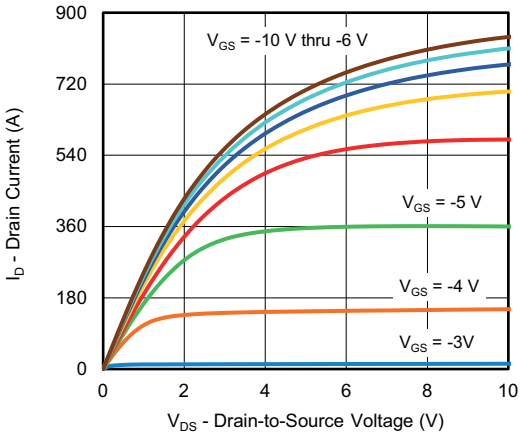
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = -250 µA		-80	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA		-1.5	-2.0	-2.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = -80 V	-	-	-1	µA
		V_{GS} = 0 V	V_{DS} = -80 V, T_J = 125 °C	-	-	-50	
		V_{GS} = 0 V	V_{DS} = -80 V, T_J = 175 °C	-	-	-150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = -10 V	V_{DS} ≥ -5 V	-30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V	I_D = -10 A	-	0.0046	0.0055	Ω
		V_{GS} = -10 V	I_D = -10 A, T_J = 125 °C	-	-	0.0098	
		V_{GS} = -10 V	I_D = -10 A, T_J = 175 °C	-	-	0.0120	
		V_{GS} = -4.5 V	I_D = -8 A	-	0.0063	0.0075	
Forward transconductance [b]	g_{fs}	V_{DS} = -15 V, I_D = -30 A		-	110	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = -25 V, f = 1 MHz	-	10 343	14 481	pF
Output capacitance	C_{oss}			-	4135	4789	
Reverse transfer capacitance	C_{rss}			-	196	275	
Total gate charge [c]	Q_g	V_{GS} = -10 V	V_{DS} = -40 V, I_D = -50 A	-	153	230	nC
Gate-source charge [c]	Q_{gs}			-	39	-	
Gate-drain charge [c]	Q_{gd}			-	20	-	
Gate resistance	R_g	f = 1 MHz		0.8	1.8	3.2	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -40 V, R_L = 4 Ω, I_D ≅ -10 A, V_{GEN} = -10 V, R_g = 1 Ω		-	19	29	ns
Rise time [c]	t_r			-	11	17	
Turn-off delay time [c]	$t_{d(off)}$			-	80	120	
Fall time [c]	t_f			-	21	32	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	-619	A
Forward voltage	V_{SD}	I_F = -10 A, V_{GS} = 0 V		-	-0.76	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -40 A, di/dt = 100 A/µs		-	105	210	ns
Body diode reverse recovery charge	Q_{rr}			-	205	410	nC
Reverse recovery fall time	t_a			-	56	-	ns
Reverse recovery rise time	t_b			-	52	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	-3.1	-	A

Notes

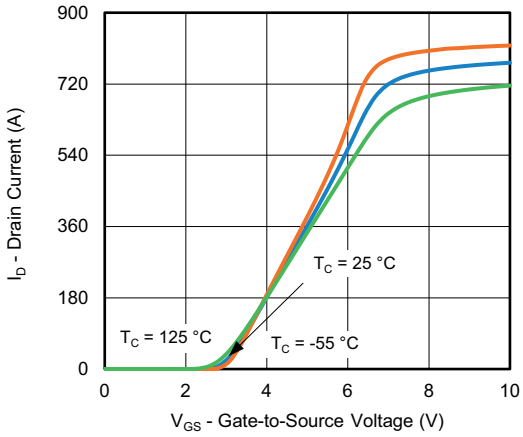
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

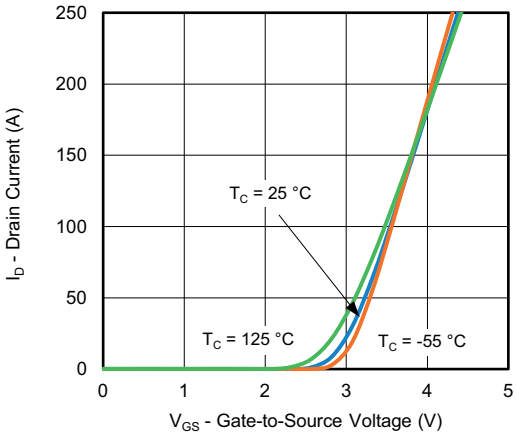
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



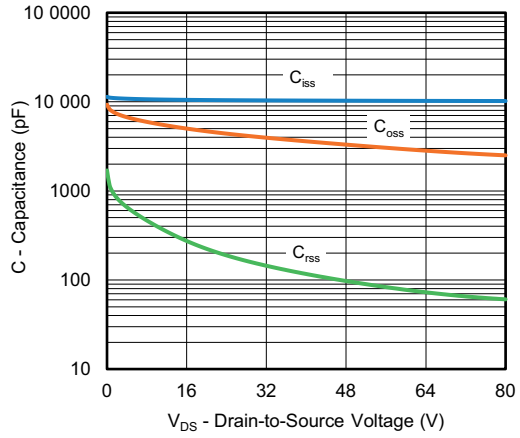
Output Characteristics



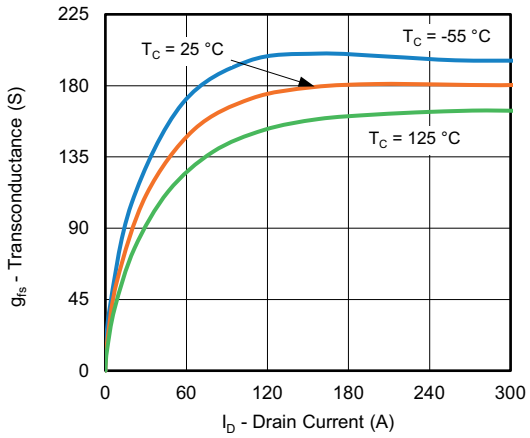
Transfer Characteristics



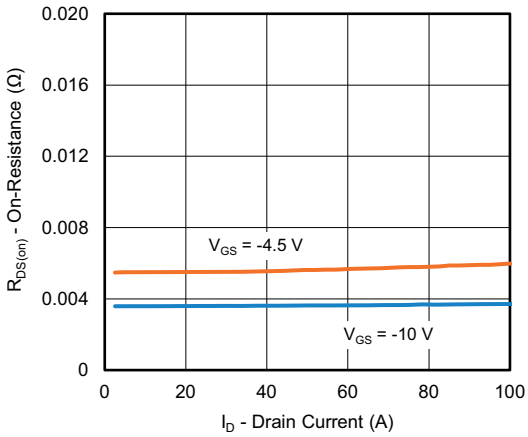
Transfer Characteristics



Capacitance

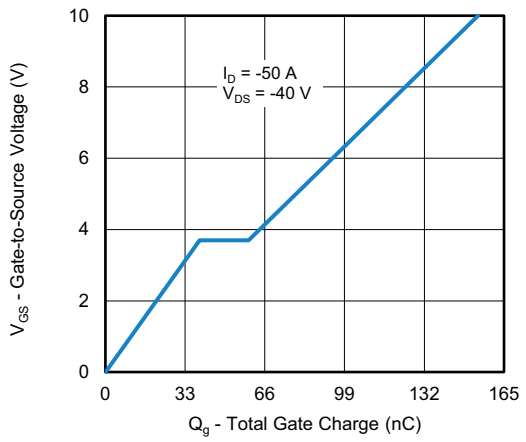


Transconductance

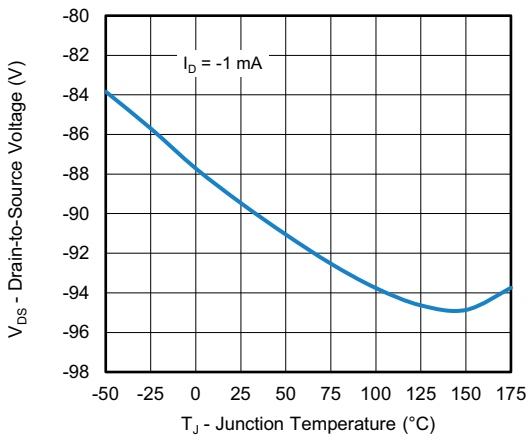


On-Resistance vs. Drain Current

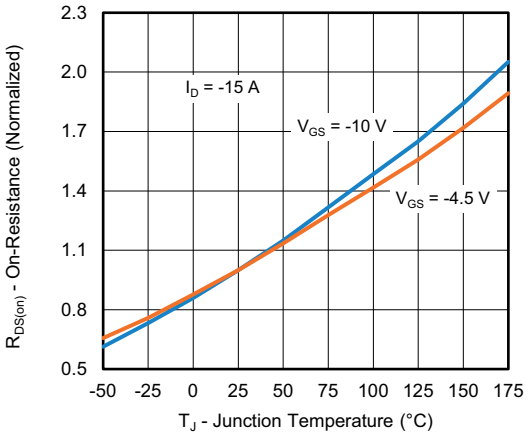
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



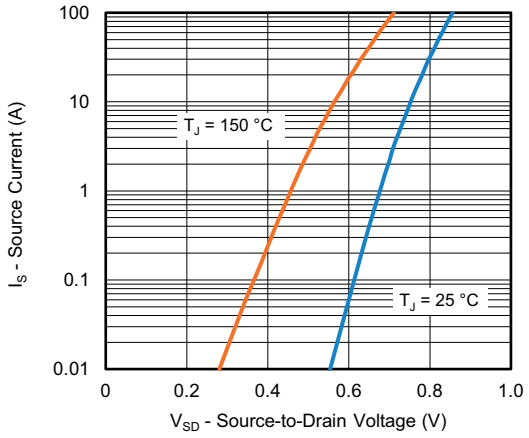
Gate Charge



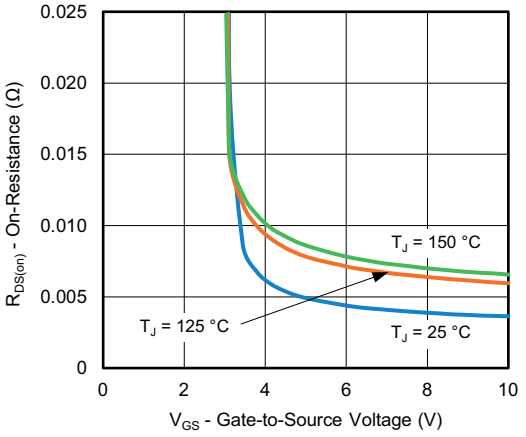
Drain-Source Breakdown vs. Junction Temperature



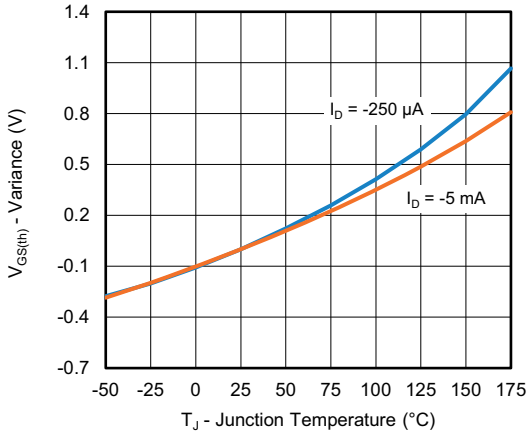
On-Resistance vs. Junction Temperature



Source Drain Diode Forward Voltage

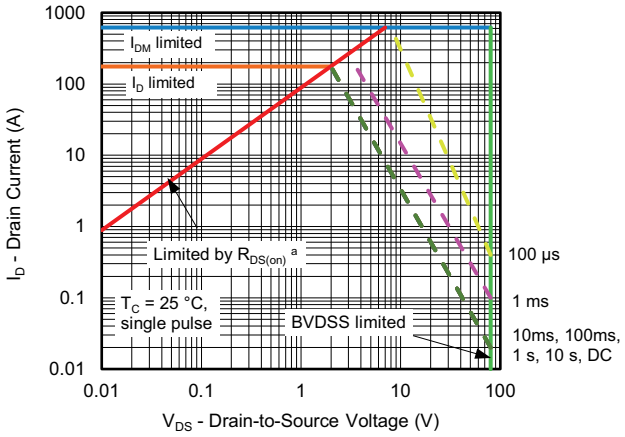


On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

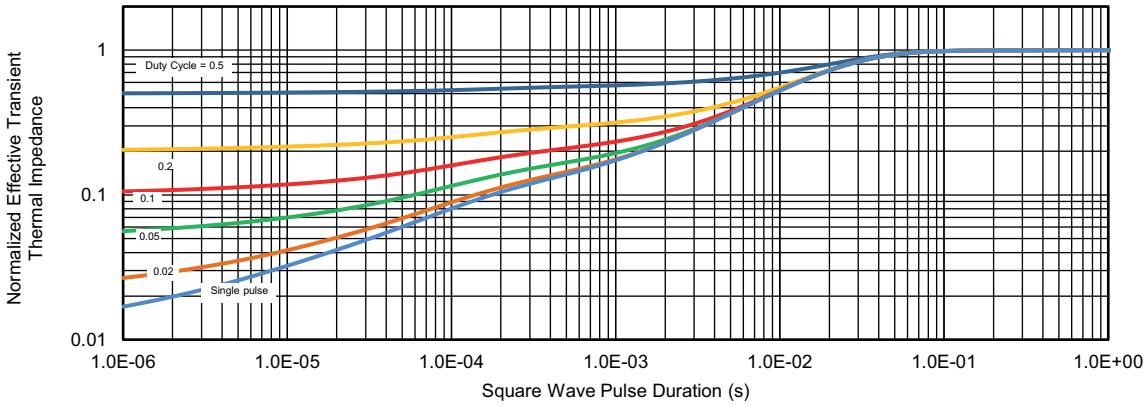


Safe Operating Area

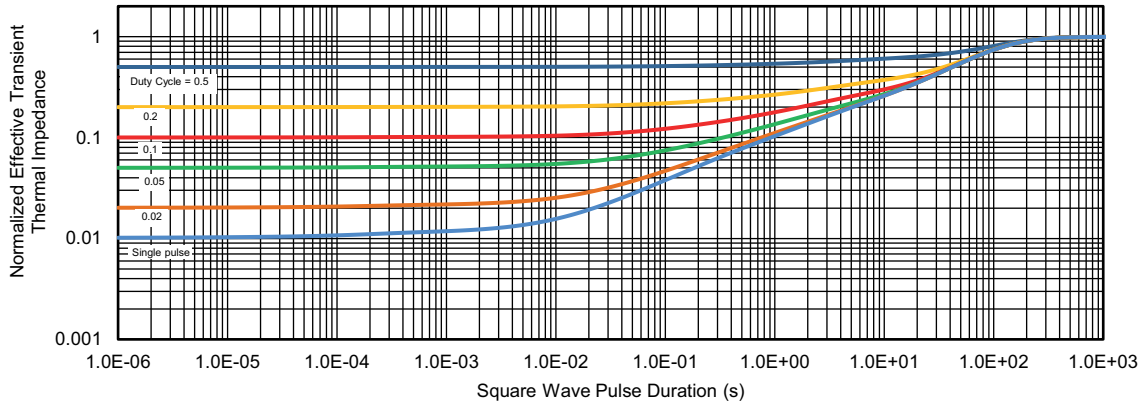
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

THERMAL RATINGS (T_C = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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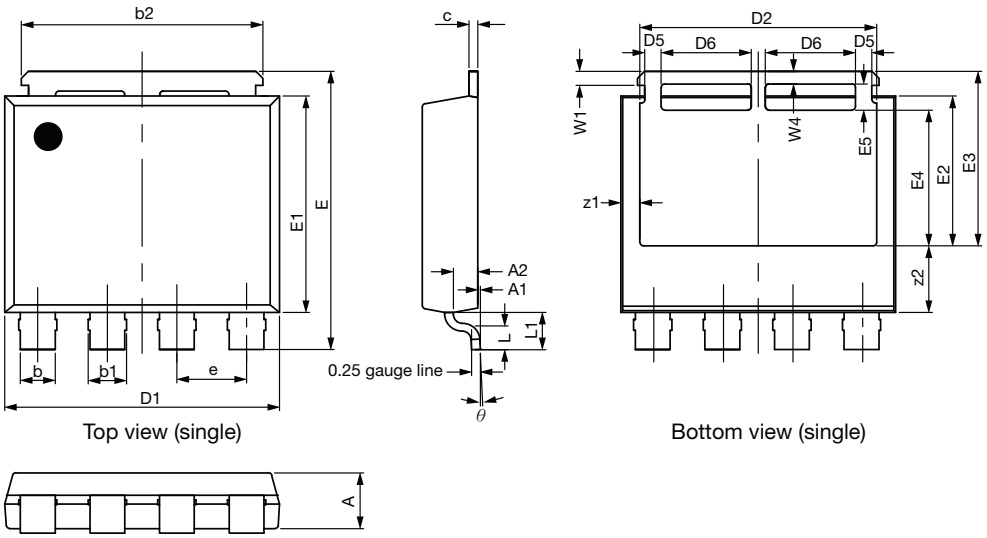
PowerPAK® 8 x 8L BWL Case Outline 2



Top view (single)

Bottom view (single)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°
ECN: S19-0643-Rev. B, 05-Aug-2019 DWG: 6073						

Note

- Millimeter will govern

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