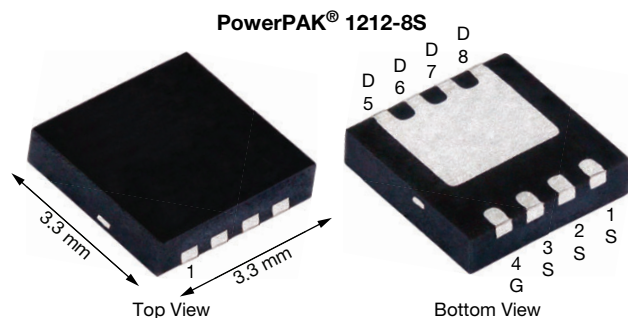


P-Channel 20 V (D-S) MOSFET



FEATURES

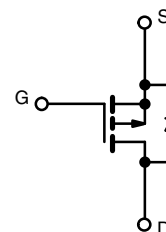
- TrenchFET® Gen V p-channel power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- Battery management
- Motor drive control



P-Channel MOSFET

PRODUCT SUMMARY

V _{DS} (V)	-20
R _{DS(on)} max. (Ω) at V _{GS} = -10 V	0.0022
R _{DS(on)} max. (Ω) at V _{GS} = -4.5 V	0.00275
R _{DS(on)} max. (Ω) at V _{GS} = -2.5 V	0.0042
Q _g typ. (nC) at V _{GS} = -4.5 V	64
I _D (A)	-136.7
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK® 1212-8S
Lead (Pb)-free and halogen-free, BLR and IOL	SiSS5207DN-T1-UE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	-20	V
Gate-source voltage	V _{GS}	± 12	V
Continuous drain current (V _{GS} = -10 V, T _J = 150 °C)	I _D	T _C = 25 °C	-136.7
		T _C = 70 °C	-109.3
		T _A = 25 °C	-38.7 ^{a, b}
		T _A = 70 °C	-30.7 ^{a, b}
Pulsed drain current (t = 100 μs)	I _{DM}	-500	A
Continuous source-drain diode current	I _S	T _C = 25 °C	-59.8
		T _A = 25 °C	-4.7 ^{a, b}
Single pulse avalanche current	I _{AS}	-20	A
Single pulse avalanche energy	E _{AS}	20	mJ
Maximum power dissipation	P _D	T _C = 25 °C	65.7
		T _C = 70 °C	42.1
		T _A = 25 °C	5.2 ^{a, b}
		T _A = 70 °C	3.3 ^{a, b}
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^{c, d}		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{a, e}	R _{thJA}	20	24	°C/W
Maximum junction-to-case (drain)	R _{thJC}	1.5	1.9	°C/W

Notes

- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK® 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 64 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = -1 mA	-20	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = -1 mA	-	-16.4	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = -250 μA	-	3.7	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-0.5	-	-1.5	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	-	-	100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μA
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -20 A	-	0.0018	0.0022	Ω
		V _{GS} = -4.5 V, I _D = -20 A	-	0.0022	0.00275	
		V _{GS} = -2.5 V, I _D = -20 A	-	0.0032	0.0042	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -20 A	-	140	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	-	10 125	-	pF
Output capacitance	C _{oss}		-	1000	-	
Reverse transfer capacitance	C _{rss}		-	900	-	
Total gate charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -20 A	-	139	210	nC
Gate-source charge	Q _{gs}	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -20 A	-	64	100	
Gate-drain charge	Q _{gd}		-	15.5	-	
			-	15.2	-	
Gate resistance	R _g	f = 1 MHz	2.5	5.0	9	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 1.0 Ω, I _D ≅ -20 A, V _{GEN} = -10 V, R _g = 1 Ω	-	12	24	ns
Rise time	t _r		-	6	12	
Turn-off delay time	t _{d(off)}		-	180	360	
Fall time	t _f		-	90	180	
Turn-on delay time	t _{d(on)}	V _{DD} = -10 V, R _L = 1.0 Ω, I _D ≅ -20 A, V _{GEN} = -4.5 V, R _g = 1 Ω	-	26	56	
Rise time	t _r		-	75	150	
Turn-off delay time	t _{d(off)}		-	150	300	
Fall time	t _f		-	100	200	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-59.8	A
Pulse diode forward current	I _{SM}		-	-	-500	
Body diode voltage	V _{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.64	-1.1	V
Body diode reverse recovery time	t _{rr}	I _F = -10 A, di/dt = 100 A/μs, T _J = 25 °C	-	23	46	ns
Body diode reverse recovery charge	Q _{rr}		-	13	26	nC
Reverse recovery fall time	t _a		-	13	-	ns
Reverse recovery rise time	t _b		-	10	-	

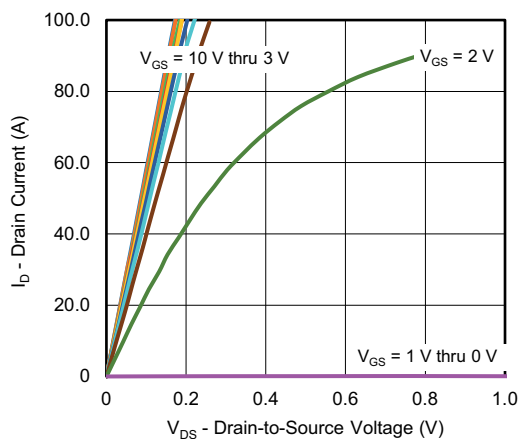
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

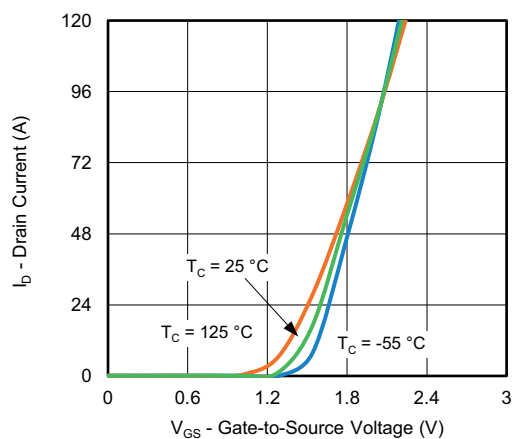
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



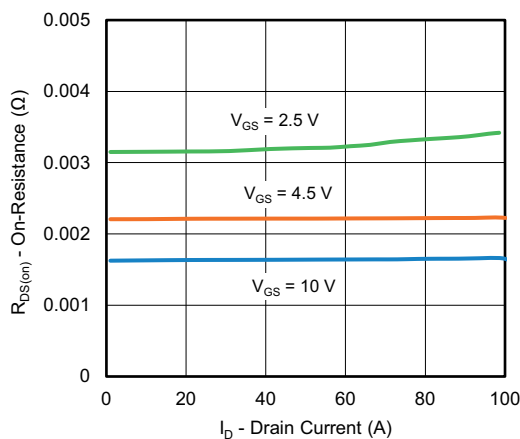
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



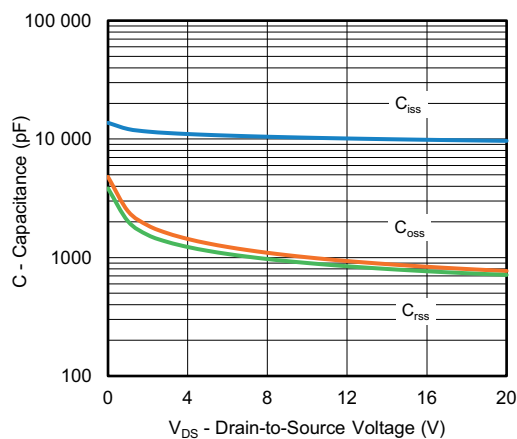
Output Characteristics



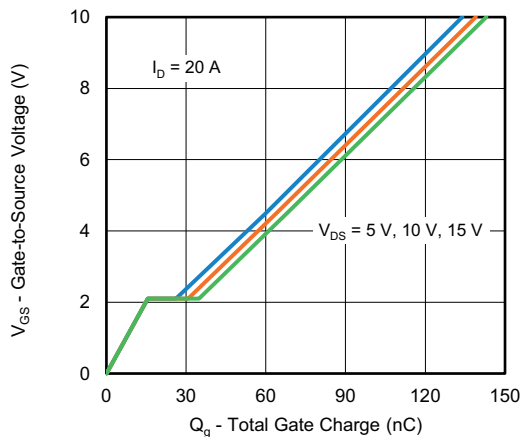
Transfer Characteristics



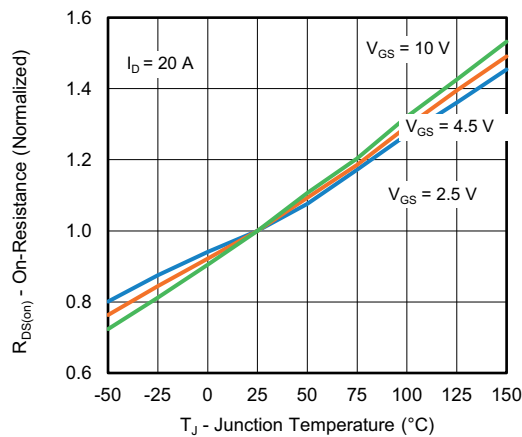
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



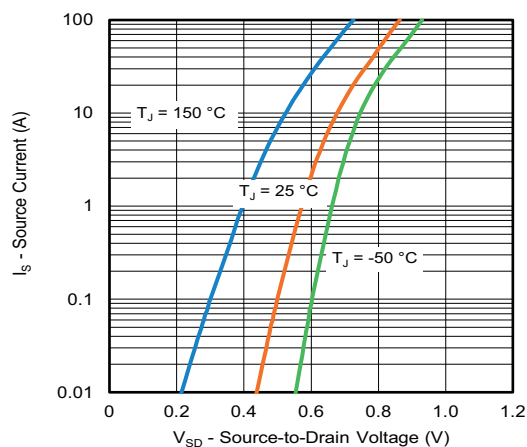
Gate Charge



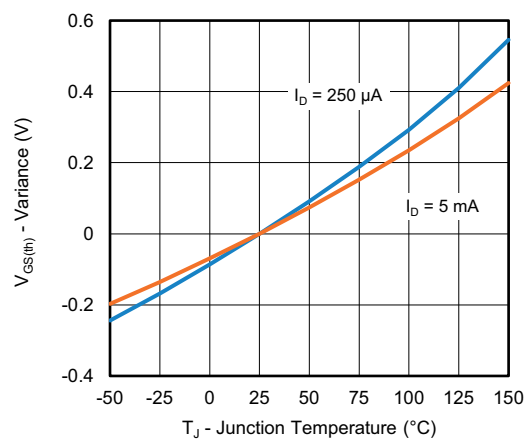
On-Resistance vs. Junction Temperature



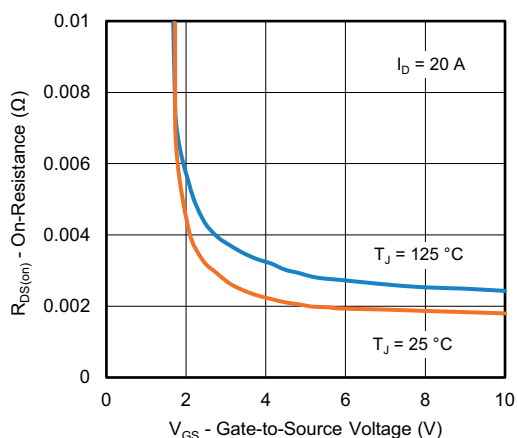
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



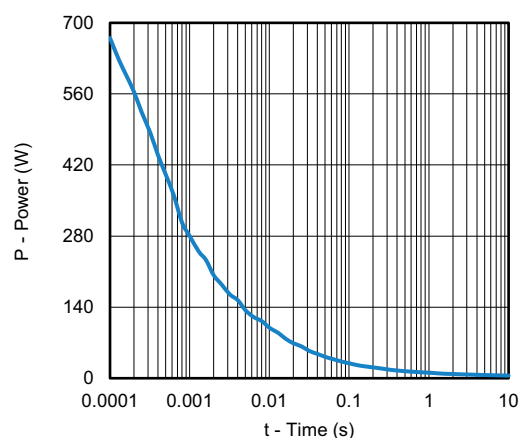
Source-Drain Diode Forward Voltage



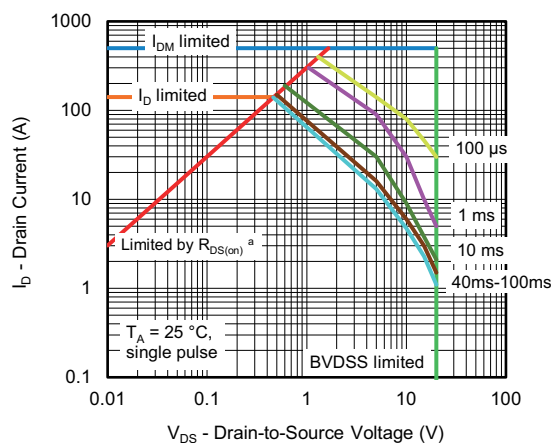
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



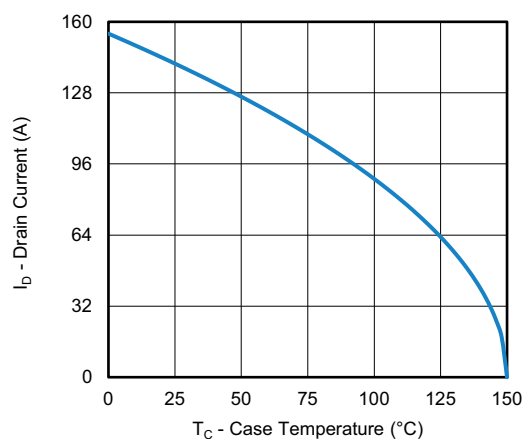
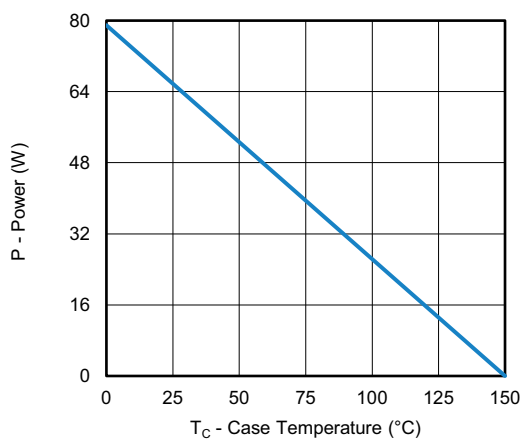
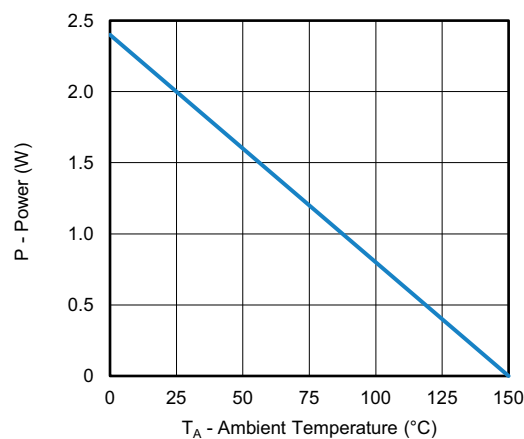
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Case

Note

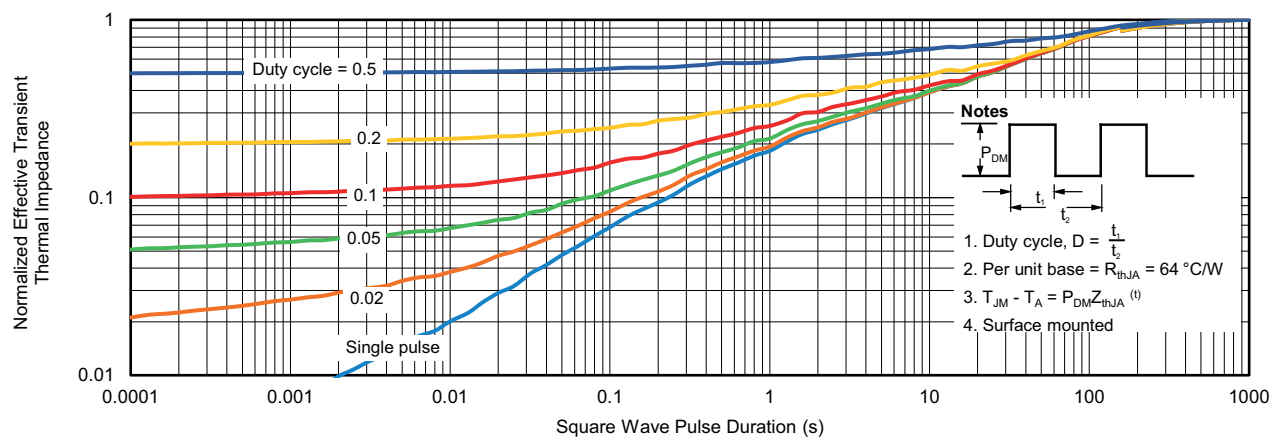
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

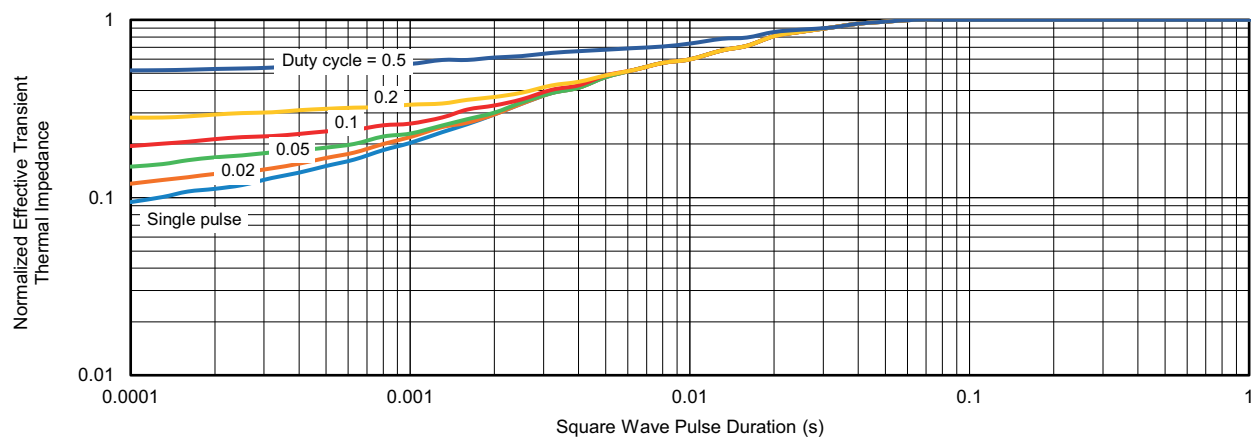
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



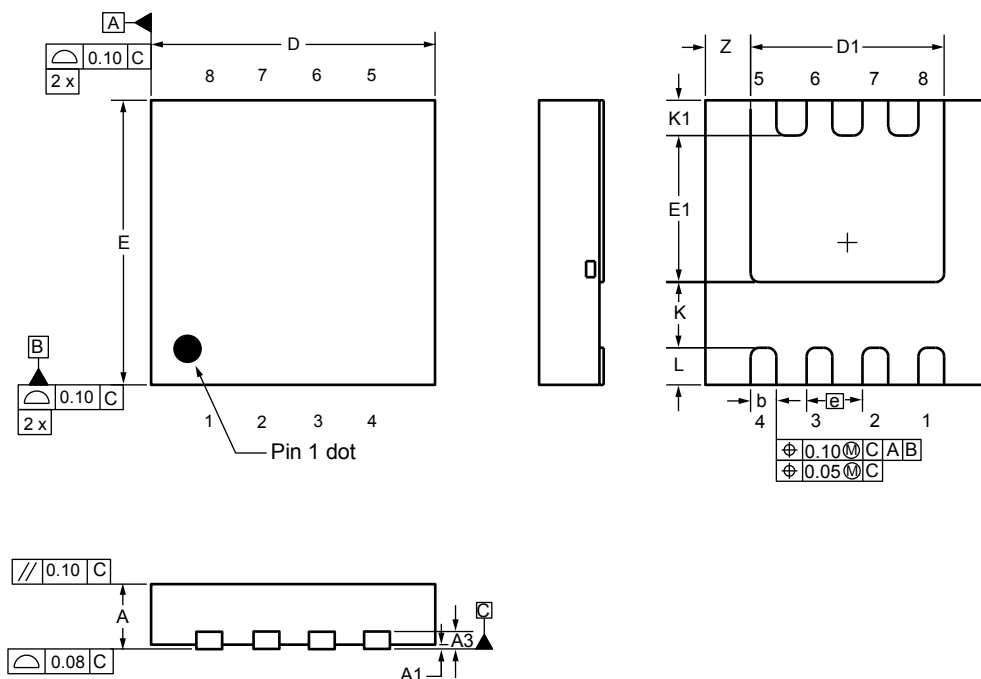
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

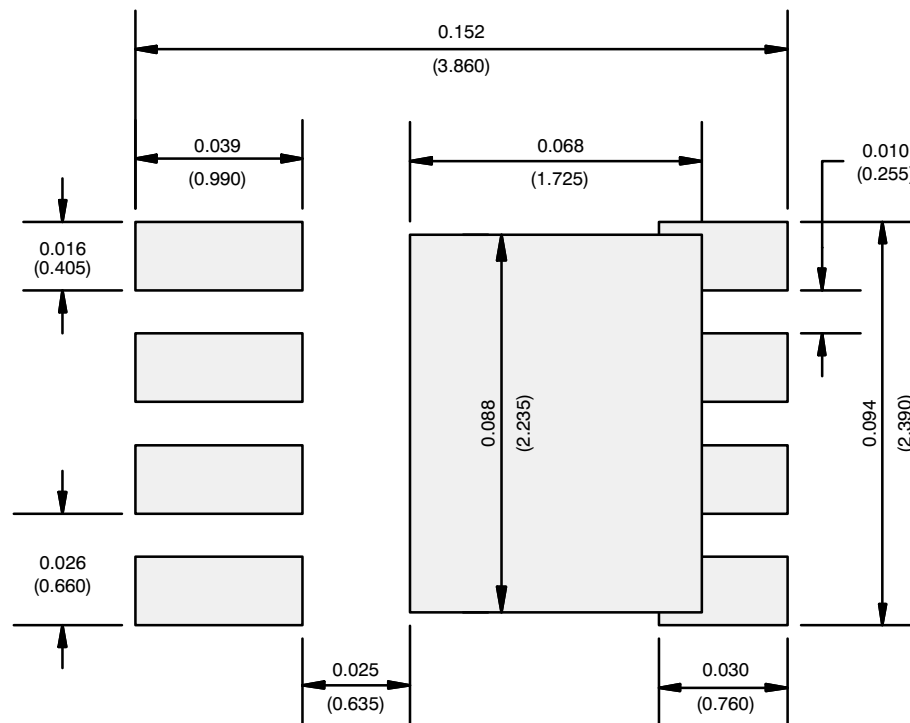
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Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: C20-0862-Rev. B, 20-Jul-2020						
DWG: 6008						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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