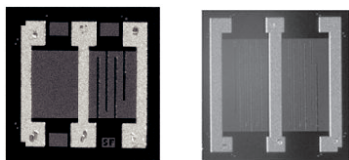


Thin Film Resistor Divider Network on Silicon, User Trimmable



Product may not be to scale

The SC7 and SCB series resistor chips offer a combination of nichrome user trimmability as a single resistor or as a ratio trim while maintaining the excellent TCR tracking characteristics of two resistors on the same chip. The SC7 and SCBs are manufactured using Vishay Electro-Films (EFI) sophisticated thin film equipment and manufacturing technology. The SC7 and SCBs are 100 % electrically tested and visually inspected to MIL-STD-883, method 2032 class H or class K.

FEATURES

- Wire bondable
- Chip size
SC7 - 0.030" x 0.030"
SCB - 0.050" x 0.050"
- Resistance range R_T :
100 Ω to 20 k Ω for SC7
100 Ω to 50 k Ω for SCB
- Case: 0303, 0505
- Silicon substrate
- Power: 250 mW or 400 mW capability
- Resistor material: Nichrome
- User trimmable
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

APPLICATIONS

Vishay EFI SC7 and SCB chip resistors have excellent power dissipation capability and are ideally suited for prototyping.

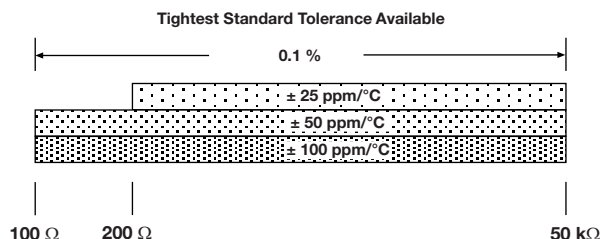
Typical application areas are:

- Amplifiers
- Oscillators
- Attenuators
- Couplers
- Filters

Recommended for hermetic environments where die is not exposed to moisture

TEMPERATURE COEFFICIENT OF RESISTANCE, VALUES, AND TOLERANCES

PARAMETER	VALUE	UNIT
Total Resistance Range	100 to 50K	Ω
Standard Tolerances	± 0.1	%
TCR	$\pm 25, \pm 50, \pm 100$	ppm/ $^{\circ}$ C



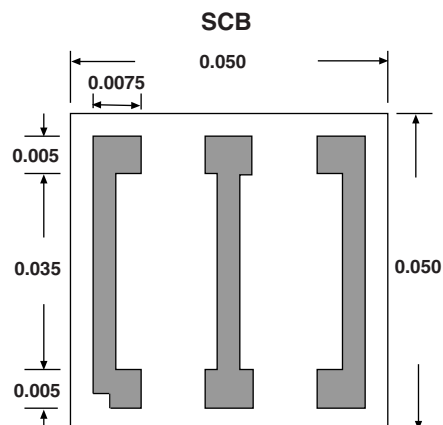
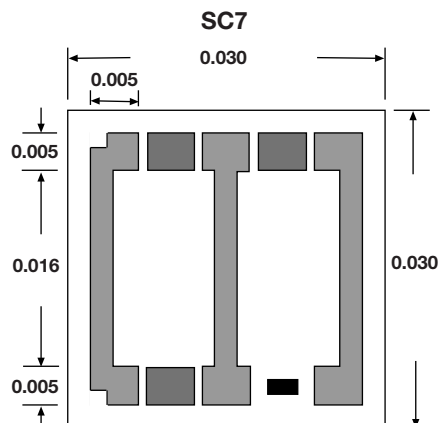
STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	VALUE	UNIT
Noise, MIL-STD-202, Method 308	- 20 typ.	dB
Stability, 1000 h, + 125 $^{\circ}$ C at Rated Power	+ 0.1 max. $\Delta R/R$	%
Operating Temperature Range	- 55 to + 125	$^{\circ}$ C
Thermal Shock, MIL-STD-202, Method 107, Test Condition F	+ 0.25 max. $\Delta R/R$	%
High Temperature Exposure, + 150 $^{\circ}$ C, 100 h	+ 0.25 max. $\Delta R/R$	%
Dielectric Voltage Breakdown	400	V
Insulation Resistance	10^{12} min.	Ω
Operating Voltage	100 max.	V
DC Power Rating at 70 $^{\circ}$ C	0.25 max. (0.030")	W
Derating to Zero at 150 $^{\circ}$ C	0.4 max. (0.050")	
5 x Rated Power Short-Time Overload, + 25 $^{\circ}$ C, 5 s	+ 0.25 max. $\Delta R/R$	%

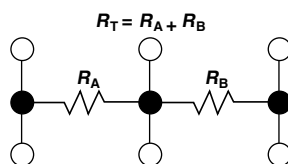
Note

- Performance characteristics are not guaranteed once user trimmed

DIMENSIONS in inches



SCHEMATIC



MECHANICAL SPECIFICATIONS

PARAMETER	VALUE
Chip Size	0.030" x 0.030" ± 0.003" (0.76 mm x 0.76 mm ± 0.076 mm) 0.050" x 0.050" ± 0.003" (1.27 mm x 1.27 mm ± 0.076 mm)
Chip Thickness	0.010" ± 0.002" (0.25 mm ± 0.05 mm)
Chip Substrate Material	Oxidized silicon, 10 kÅ minimum SiO ₂
Resistor Material	Nichrome
Bonding Pad Size	0.005" x 0.005" (0.127 mm x 0.127 mm) min.
Number of Pads	6
Pad Material	15 kÅ minimum gold standard
Backing	None, lapped semiconductor silicon

GLOBAL PART NUMBER INFORMATION

Global Part Number: SC750000KCKKGNHWS

Global Part Number Description: SC7 5K 10 % RT 0.25 % 100 ppm/°C 10 ppm/°C Au None H WS

S	C	7	5	0	0	0	0	K	C	K	K	G	N	H	W	S
MODEL	RESISTANCE (R TOTAL)	RESISTANCE MULTIPLIER CODE	TOL. CODE (%)	RATIO TOL. (%)	TCR (ppm/°C)	TC TRACK (ppm/°C)	TERMINATION	BACK METAL	VISUAL CLASS	PACKAGING CODE						
SC7 = 30 x 30 size SCB = 50 x 50 size	First 4 digits are significant figures of resistance	B = 0.01 A = 0.1 0 = 1 1 = 10	B = 0.1 C = 0.25 D = 0.5 F = 1.0 G = 2.0 J = 5.0 K = 10	B = 0.1 C = 0.25 D = 0.5 F = 1.0 G = 2.0 U = User N = No	E = ± 25 C = ± 50 K = ± 100 M = ± 250	G = ± 2 J = ± 5 K = ± 10 N = No	G = Au A = Al	G = Au N = None	H = Class H K = Class K	WS = Waffle pack 100 min., 1 mult						



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