Ceramic Disc, RFI, and Safety Capacitors

In accordance with IEC recommendations ceramic capacitors are subdivided into two classes:

- CERAMIC CLASS 1 or low-K capacitors are mainly manufactured of titanium dioxide or magnesium silicate
- CERAMIC CLASS 2 or high-K capacitors contain mostly alkaline titanate

MAIN FEATURES

	CLASS 1	CLASS 2
Application	For temperature compensation of frequency discriminating circuits and filters, coupling and decoupling in high-frequency circuits where low losses and narrow capacitance tolerances are demanded. Mainly X, and Y capacitor according to IEC 60384-14; EMI / RFI suppression and filtering.	As coupling and decoupling capacitor with reduced dimensions for such application where higher losses and a reduced capacitance stability are acceptable. Mainly X, and Y capacitor according to IEC 60384-14; EMI / RFI suppression and filtering.
Properties Temperature dependence capacitance	High stability of capacitance. Low dissipation factor up to higher frequencies. Defined temperature coefficient of capacitance, positive or negative, linear, and reversible. High insulation resistance. High long-term stability of electrical values.	High capacitance values with small dimensions. Non-linear dependence of capacitance on temperature.
DC voltage Capacitance dependence	None to low	Medium to high
Dissipation factor tan δ	Maximum 0.5 % (1 MHz)	Maximum 2.5 % (1 kHz)
Insulation resistance	$\geq 10^9\ \Omega$	$\geq 10^9\ \Omega$
Capacitance tolerances	± 10 %, ± 20 %	± 10 %, ± 20 %
Rated voltage	Up to 15 kV_{DC}	Up to 20 kV_{DC}

STANDARD SPECIFICATIONS

GENERAL STANDARDS	
IEC 60062	Marking codes for resistors and capacitors
IEC 60068	Basic environmental testing procedures
SPECIAL STANDARDS FOR CERAMIC CAPACITORS	
EN 130600 and IEC 60384-8	Fixed capacitors of ceramic dielectric, class 1
EN 130700 and IEC 60384-9	Fixed capacitors of ceramic dielectric, class 2
STANDARDS FOR SPECIAL APPLICATION PURPOSES	
IEC 60384-14	RFI and safety capacitors
DIN EN 60384-14	
UL 60384-14	
CSA E60384-14	

MEASURING AND TESTING CONDITIONS

	CLASS 1	CLASS 2
Capacitance and dissipation factor	C ≥ 1000 pF 1 kHz, 1.0 V_{RMS} to 5 V_{RMS} C < 1000 pF 1 MHz, 1.0 V_{RMS} to 5 V_{RMS}	C ≥ 100 pF 1 kHz, 1.0 V_{RMS} ± 0.2 V_{RMS} C < 100 pF 1 MHz, 1.0 V_{RMS} ± 0.2 V_{RMS}
Insulation resistance	Rated voltage < 100 V: ≥ 100 V to < 500 V: ≥ 500 V: Measuring time:	measuring voltage = 10 V ± 1 V measuring voltage = 100 V ± 15 V measuring voltage = 500 V ± 50 V 60 s ± 5 s
Dielectric strength	Rated voltage: ≤ 500 V: > 500 V: Testing time:	test voltage = 2.5 x U_R test voltage = 1.5 x U_R 2 s

Note

- Climatic test conditions: Temperature 20 °C to 25 °C
  Relative humidity 50 % to 70 %

MARKING

See individual datasheet.

CAPACITANCE CODING SYSTEM			
CAPACITANCE VALUE	**CODE**	**CAPACITANCE VALUE**	
	33p	33 pF	
	330p	330 pF	
	n33	330 pF (0.33 nF)	
	3n3	3300 pF (3.3 nF)	
	33n	33 000 pF (33 nF)	
	330n	330 000 pF (330 nF)	
	µ33	0.33 µF	
	3µ3	3.3 µF	
CAPACITANCE TOLERANCE	**CODE LETTER**	**C-TOLERANCE < 10 pF (pF)**	**C-TOLERANCE ≥ 10 pF (%)**
	K	-	± 10
	M	-	± 20
RATED VOLTAGE	Clear text		

PRODUCTION CODE ACCORDING TO IEC 60062

The production code is indicated with a 4 digit code.

4 DIGIT CODE (YEAR / WEEK)

The 1st two digits indicate the year and the second two digits indicate the week.

Example

19th week 2025 = 2519

CODING OF THE TEMPERATURE CHARACTERISTIC OF CAPACITANCE FOR CLASS 2 CERAMIC CAPACITORS

ACCORDING TO EIA STANDARD RS 198

Y — Lower category temperature

5 — Upper category temperature

S — Admissible capacitance change related to 25 °C over the entire temperature range

TEMPERATURE	CODE LETTER
-55 °C	X
-30 °C	Y
+10 °C	Z

TEMPERATURE	CODE FIGURE
+45 °C	2
+65 °C	4
+85 °C	5
+105 °C	6
+125 °C	7

CHANGE	CODE LETTER
± 1 %	A
± 1.5 %	B
± 2.2 %	C
± 3.3 %	D
± 4.7 %	E
± 7.5 %	F
± 10 %	P
± 15 %	R
± 22 %	S
± 22 %/- 33 %	T
± 22 %/- 56 %	U
± 22 %/- 82 %	V

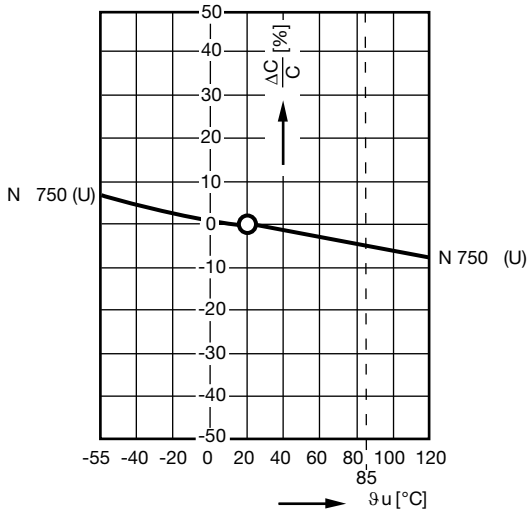
CLASS 1 CERAMIC TYPE
TEMPERATURE COEFFICIENT OF THE CAPACITANCE FOR CLASS 1 CERAMIC CAPACITORS

$$\frac{\Delta C}{C}\,[\%] = 100 \times \alpha \times \Delta\vartheta$$

ΔC = capacitance change

α = temperature coefficient in $10^{-6}/°C$

$\Delta\vartheta$ = temperature change in °C



DISSIPATION FACTOR

- For values greater than 50 pF: see datasheet
- For lower values the dissipation factor is calculated according to the type of ceramic (rated temperature coefficient) under consideration of the capacitance according to EN 130600

$+100 \leq \alpha > -750$: $1.5 \times \left(\frac{150}{C} + 7\right) \times 10^{-4}$

$+750 \leq \alpha > -1500$: $2 \times \left(\frac{150}{C} + 7\right) \times 10^{-4}$

$+1500 \leq \alpha > -3300$: $3 \times \left(\frac{150}{C} + 7\right) \times 10^{-4}$

$+3300 \leq \alpha > -5600$: $4 \times \left(\frac{150}{C} + 7\right) \times 10^{-4}$

$\alpha \geq -5600$: $5 \times \left(\frac{150}{C} + 7\right) \times 10^{-4}$

- The dissipation factor as well as the measuring method to be agreed between manufacturer and user for values lower than 5 pF.

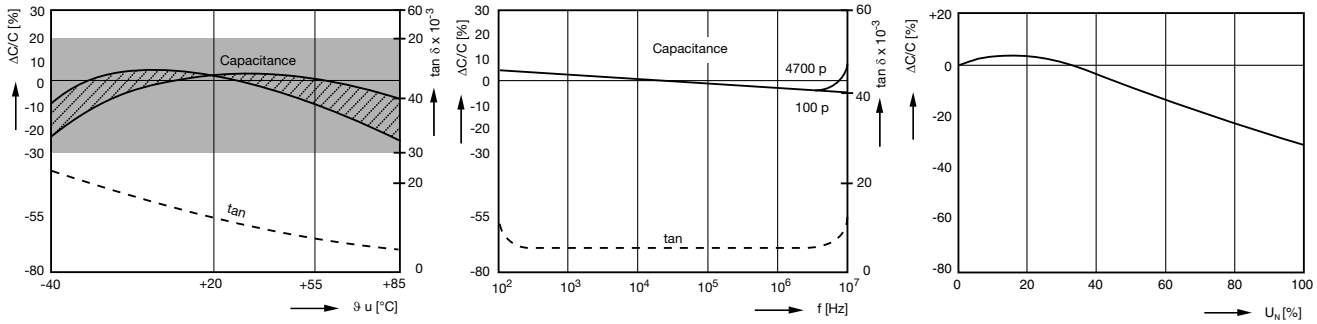
CLASS 2 CERAMIC TYPE

CAPACITANCE CHANGE AND DISSIPATION FACTOR VS. TEMPERATURE

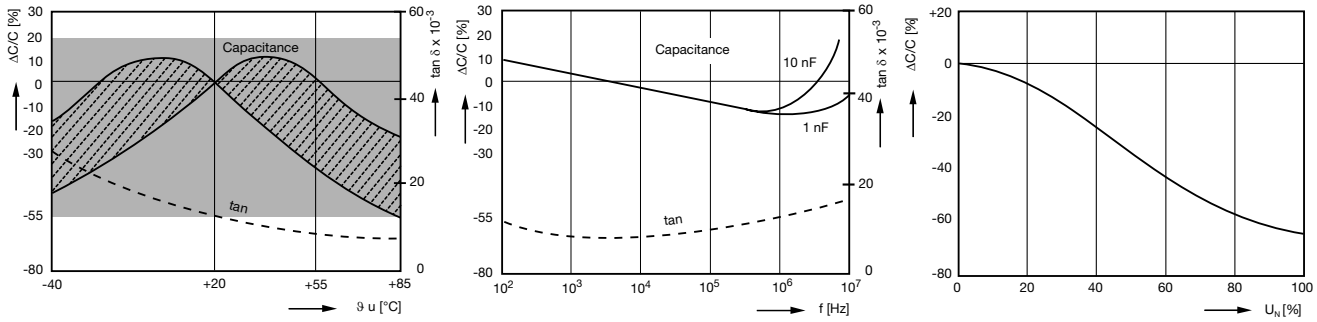
CAPACITANCE CHANGE AND DISSIPATION FACTOR VS. FREQUENCY

CAPACITANCE CHANGE VS. DC VOLTAGE

CERAMIC DIELECTRIC: Y5T



CERAMIC DIELECTRIC: Y5U



CAPACITANCE "AGING" OF CERAMIC CAPACITORS

Following the final heat treatment all class 2 ceramic capacitors reduce their capacitance value approximately according to logarithmic law due to their special crystalline construction. This change is called "aging". If the capacitors are heat treated, for example when soldering, the capacitance increases again to a higher value and the aging process begins again.

Note

- The level of this de-aging is dependent on the temperature and the duration of the heat; an almost complete de-aging is achieved at 150 °C in one hour; these conditions also form the basis for reference measurements when testing. The capacitance change per time decade (aging constant) differs for the various types of ceramic but typical values can be taken from the table below.

CERAMIC MATERIAL	Y5T	Y5U
AGING CONSTANT k	-4 %	-4 %

$$k = \frac{100 \times (C_{t1} - C_{t2})}{C_{t1} \times \log_{10}(t1/t2)}$$

t1, t2 = measuring time point (h)
C_{t1}, C_{t2} = capacitance values for the times t1, t2
k = aging constant (%)

$$C_{t2} = C_{t1} \times (1 - k/100 \times \log_{10}[t1/t2])$$

REFERENCE MEASUREMENT

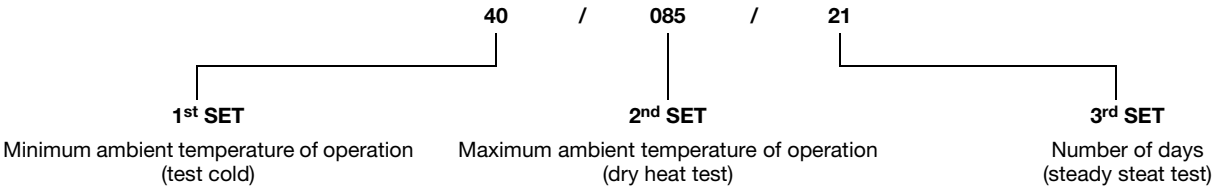
Due to aging it is necessary to specify an age for reference measurements which can be related to the capacitance with fixed tolerance. According to EN 130700 this time period is 1000 h.

If the shelf-life of the capacitor is known, the capacitance for t = 1000 h can be calculated with the aging constant.

In order to avoid the influence of the aging, it is important to de-age the capacitors before stress-testing. The following procedure is adopted (see also EN 130700):

- De-aging at 150 °C, 1 h
- Storage for 24 h at standard climatic conditions
- Initial measurement
- Stress
- De-aging at 150 °C, 1 h
- Storage for 24 h at standard climatic conditions
- Final measurement

COMPONENT CLIMATIC CATEGORY



First set: two digits denoting the minimum ambient temperature of operation (cold test).

65	-65 °C
55	-55 °C
40	-40 °C
25	-25 °C
10	-10 °C
00	0 °C
05	+5 °C

Second set: three digits denoting the maximum ambient temperature (dry heat test).

155	+155 °C
125	+125 °C
110	+110 °C
090	+90 °C
085	+85 °C
080	+80 °C
075	+75 °C
070	+70 °C
065	+65 °C
060	+60 °C
055	+55 °C

Third set: two digits denoting the number of days of the damp heat steady state test (Ca).

56	56 days
21	21 days
10	10 days
04	4 days
00	The component is not required to be exposed to damp heat

Standard coding according to IEC 60068-1.

CATEGORY EXAMPLES
25/085/04
25/085/21
40/085/21
55/125/21
55/125/56

STORAGE

The capacitors must not be stored in a corrosive atmosphere, where sulphide or chloride gas, acid, alkali or salt are present. Exposure of the components to moisture, should be avoided. The solderability of the leads is not affected by storage of up to 24 months (temperature +10 °C to +35 °C, relative humidity up to 60 %). Class 2 ceramic dielectric capacitors are also subject to aging, see previous page.

SOLDERING

SOLDERING SPECIFICATIONS		
Soldering test for capacitors with wire leads: (according to IEC 60068-2-20, solder bath method)		
	SOLDERABILITY	**RESISTANCE TO SOLDERING HEAT**
Soldering temperature	235 °C ± 5 °C	260 °C ± 5 °C
Soldering duration	2 s ± 0.5 s	10 s ± 1 s
Distance from component body	≥ 2 mm	≥ 5 mm

SOLDERING RECOMMENDATIONS

Soldering of the component should be achieved using a Sn60/40 type or a silver-bearing Sn62/36/2Ag type solder. Ceramic capacitors are very sensitive to rapid changes in temperature (thermal shock) therefore the solder heat resistance specification (see Soldering Specifications table) should not be exceeded. Subjecting the capacitor to excessive heating may result in thermal shocks that can crack the ceramic body. Similarly, excessive heating can cause the internal solder junction to melt.

CLEANING

The components should be cleaned immediately following the soldering operation with vapor degreasers.

SOLVENT RESISTANCE

The coating and marking of the capacitors are resistant to the following test method: IEC 60068-2-45 (method XA).

MOUNTING

If a defined product stop is required for mounting on a PCB, a mechanically formed product stop (kinked or inline wire) or a mounting tool should be used.

We do not recommend modifying the lead terminals, e.g. bending or cropping. This action could break the coating or crack the ceramic insert. If however, the lead must be modified in any way, we recommend support of the lead with a clamping fixture next to the coating.

AQL / FIT VALUES / SUPPLIED QUALITY

AQL 0.1 FOR THE SUM OF THE ELECTRIC MAIN FAULTS

- C-tolerance > 1.5 x tolerance limit
- DF > 1.5 x catalog value
- R_{IS} < catalog value
- Inadequate dielectric breakdown
- Interruption

AQL 0.25 FOR THE SUM OF THE MECHANICAL MAIN FAULTS

- Marking wrong or missing
- Dimensions out of tolerance
- Coating failure
- Lead space out of tolerance
- Poor solderability of leads
- Wrong lead length

AQL 0.65 FOR SECONDARY FAULTS

- Coating extension out of tolerance
- Marking incomplete
- Tape dimensions out of tolerance
- Testing in accordance to IEC 60410

Notes

The following agreements are possible on request:

- Lower AQL values
- Confirmed initial random sampling test with appropriate report
- Report on production test findings
- Agreement on ppm concept

RELIABILITY

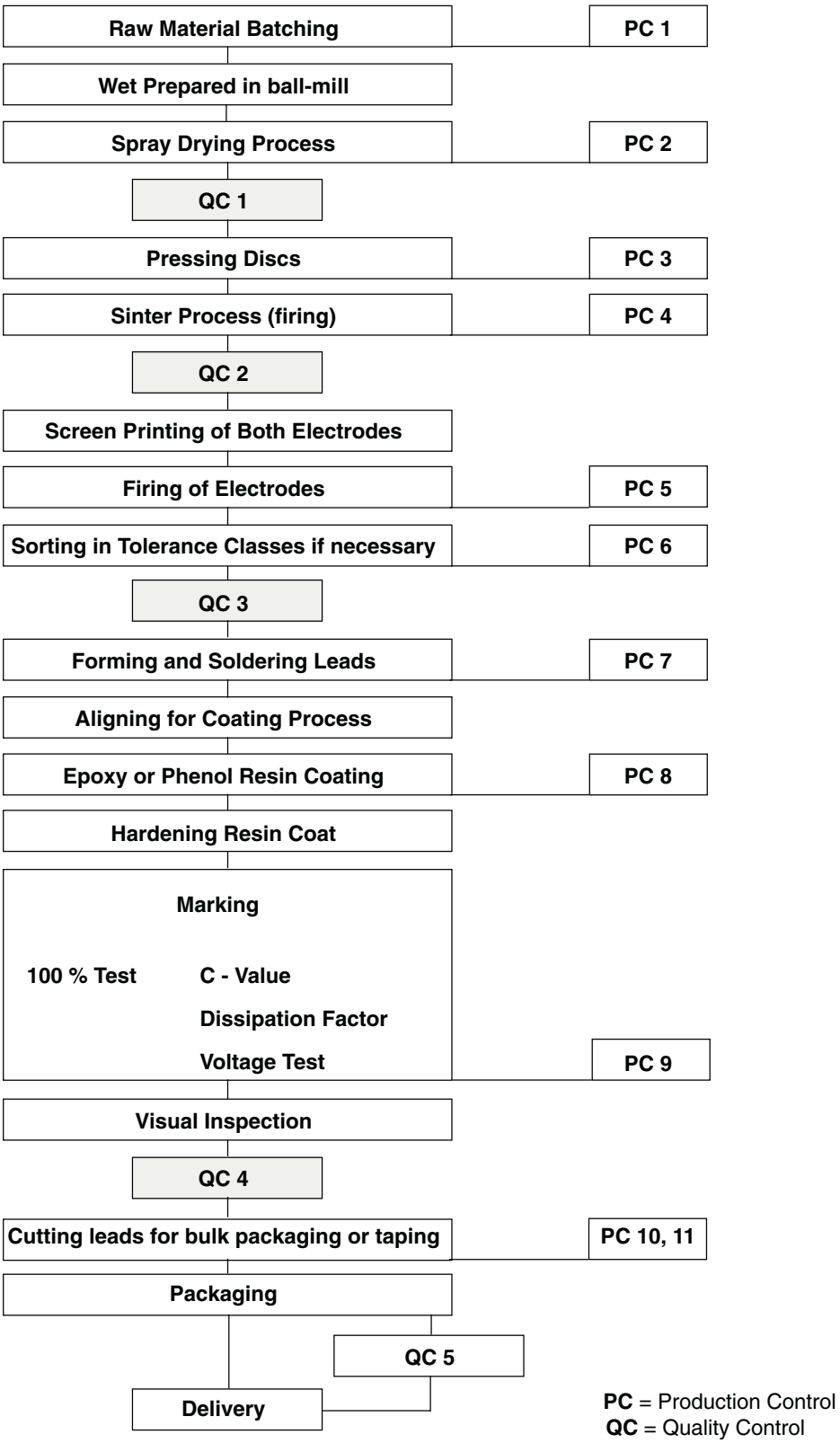
By careful control of the manufacturing process stages, the quality of the product is maintained at the highest possible level. To obtain data on the reliability of our ceramic capacitors, many long-term tests under increased temperature and voltage conditions have been carried out in our laboratories.

Based on the results of these tests, the following can be stated:

Reference conditions:	Ambient temperature:	40 °C ± 2 °C
	Relative humidity:	60 % ± 2 %
	Electrical stress:	50 % rated voltage (U_R)
Failure criteria:	Short circuit ($R \leq 10^{-5}\ \Omega$) or open circuit	
Failure tests:	Class 1 capacitors:	$\lambda = 2 \times 10^{-9}\ h^{-1}$
	Class 2 capacitors:	$\lambda = 5 \times 10^{-9}\ h^{-1}$

By derating the voltage load, greatly increased reliability can be predicted.
Temperature, up to the maximum category temperature, is not believed to significantly affect the reliability.

PRODUCTION FLOWCHART



AVAILABLE STANDARD LEAD CONFIGURATIONS

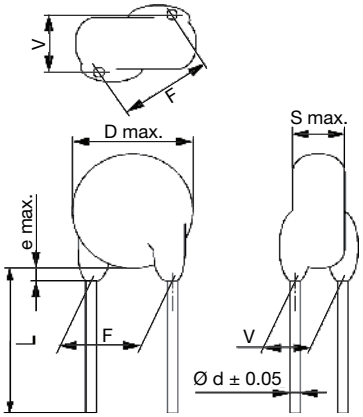
FORM 1

STRAIGHT LEAD

e	3.0 MAX.
L	30 - 3 or 10 ± 1

d	0.6 or 0.8
F	5.0*) / 7.5 / 10 / 12.5

*) only when d = 0.6

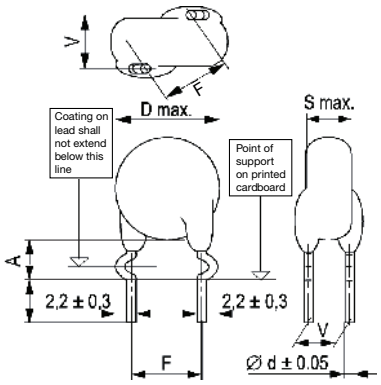


FORM 2

OUTSIDE CRIMP

F	d	A ± 1
5.0*)	0.6	5.0
7.5	0.6	5.0
7.5	0.8	6.0
10	0.6	6.0
10	0.8	6.0
12.5	0.6	6.0
12.5	0.8	6.0

*) only when d = 0.6

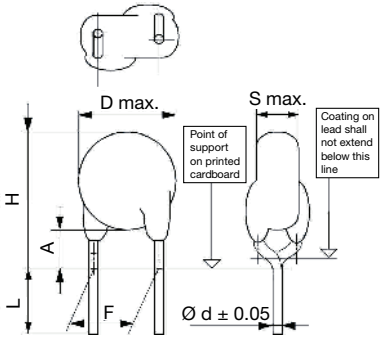


FORM 3

INLINE WIRE

F	d	A
5.0	0.6	4.5 MAX.
7.5	0.6	4.5 MAX.
10	0.8	6.0 MAX.
12.5	0.8	6.0 MAX.

F	L
7.5	2.8 MIN.
10	3.0 MIN.
12.5	3.0 MIN.



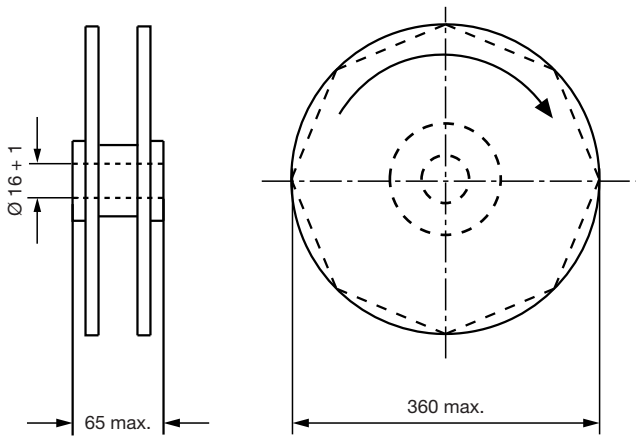
Note

- If a defined product stop is required for mounting on a PCB, a mechanically formed product stop (kinked or inline wire) or a mounting tool should be used

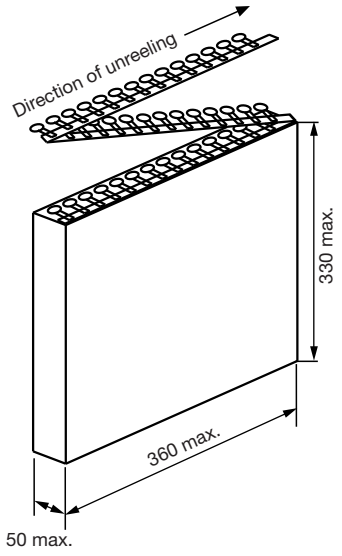
RADIAL TAPING OF CERAMIC DISC CAPACITORS			
DESIGNATION	**SYMBOL**	**TAPING T**	**TAPING F**
Pitch of component	P	12.7 ± 1	25.4 ± 1
Pitch of sprocket hole	P_0	12.7 ± 0.3	12.7 ± 0.3
Distance, hole to lead	P_1	3.85 ± 0.7	(0.5F) ± 0.7
Distance, hole to center of component	P_2	6.35 ± 1.3	12.7 ± 1.3
Lead spacing	F	5.0 / 7.5 + 0.8 / - 0.2	7.5 / 10 / 12.5 ± 0.8
Average deviation across tape	Δh	± 2.0 max.	± 3.0 max.
Average deviation in direction of reeling	Δp	± 1.3 max.	± 1.3 max.
Carrier tape width	W	18.0 + 1 / - 0.5	18.0 + 1 / - 0.5
Hold-down tape width	W_0	6	6
Position of sprocket hole	W_1	9.0 + 0.75 / - 0.5	9.0 + 0.75 / - 0.5
Distance of hold-down tape	W_2	3.0 max.	3.0 max.
Distance between the abscissa and the bottom plane of the component body (straight leads)	H	18.0 + 2 / - 0	18.0 + 2 / - 0 20.0 ± 1
Distance between the abscissa and the reference plane of the component with crimped leads (kinked leads)	H_0	16.0 ± 0.5	16.0 ± 0.5
Length of cut leads	L	11.0 max.	11.0 max.
Diameter of sprocket hole	D_0	4.0 ± 0.2	4.0 ± 0.2
Total tape thickness	t	0.9 max.	0.9 max.

PACKAGING VERSIONS

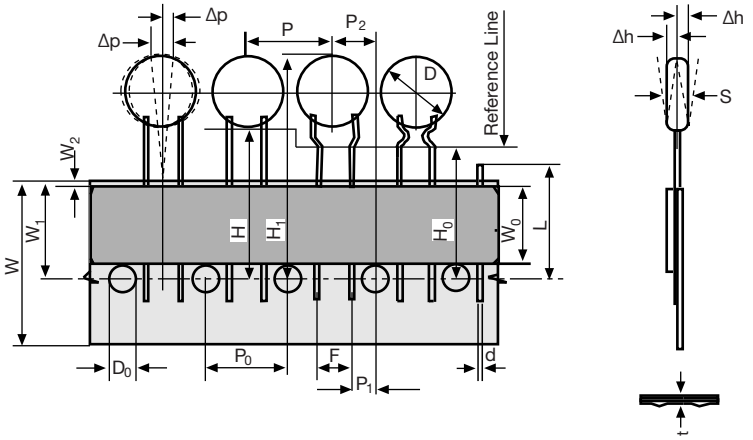
Reel Packaging



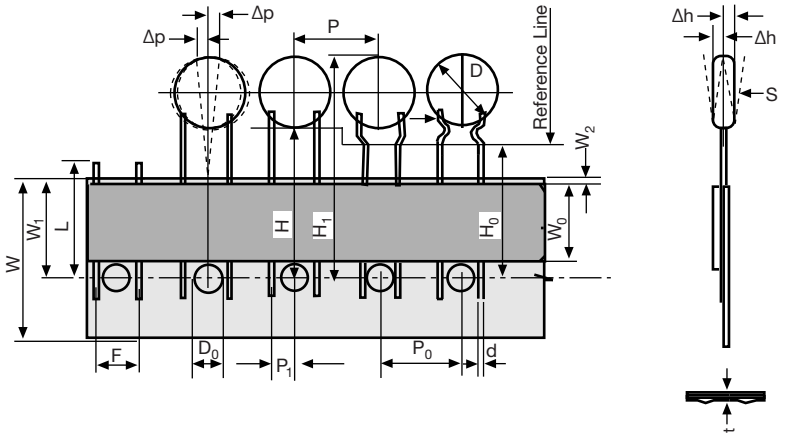
Ammo Packaging



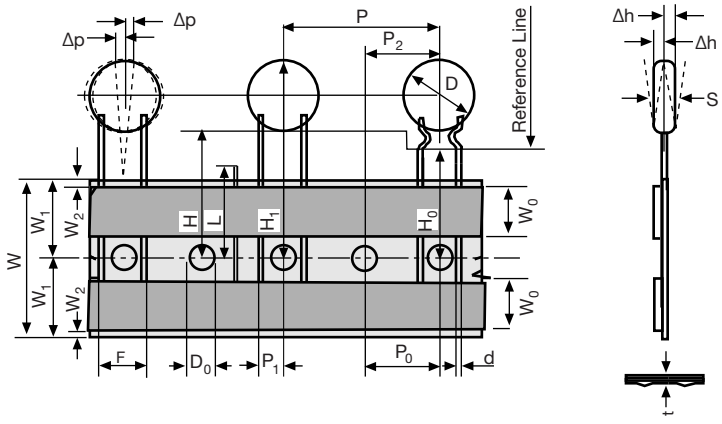
TAPING T
COMPONENT PITCH 0.5"
LEAD SPACING 5.0 mm



TAPING T
COMPONENT PITCH 0.5"
LEAD SPACING 7.5 mm



TAPING F
COMPONENT PITCH 1.0"
LEAD SPACING 7.5 mm, 10 mm, 12.5 mm



- Pulling force from the tape ≥ 5 N
- Tensile strength of tape ≥ 15 N
- Unreeling force of tape from reel ≥ 2.5 N

Maximum 0.5 % of all components on reel may be missing. A maximum of 3 consecutive components may be missing provided this gap is followed by 6 consecutive components. The splices shall have the same minimum strength as the tape. The splices must be not thicker than 1.5 mm, the sprocket holes may not be effected.

ORDER CODE, 10th, 11th AND 12th DIGIT - POSSIBLE LEAD AND PACKAGING COMBINATIONS

BULK PACKAGING						
	LEAD LENGTH L	LEAD DIA. d	LEAD SPACING F			
			5 mm	7.5 mm	10 mm	12.5 mm
Straight leads	30 mm - 3 mm	0.6 mm	BF0	CF0	DF0	EF0
		0.8 mm	-	CJ0	DJ0	EJ0
Preformed leads outside crimp	5 mm ± 1 mm	0.6 mm	TA0	TC0	TE0	TG0
		0.8 mm	-	TD0	TF0	TH0
Inline wire	Min. 2.8 mm + 1.5 mm	0.6 mm	YA0	YC0	YE0	YG0
	Min. 3.0 mm + 2.0 mm	0.8 mm	YB0	YD0	YF0	YH0

REEL PACKAGING COMPONENT PITCH 12.7 mm		
	TAPING T	
Lead diameter 0.6 mm	H = 18.0 mm straight leads only H_0 = 16.0 mm preformed leads only	
Lead spacing F	5 mm	7.5 mm
Body diameter D	Valid for ≤ 12 mm standard (> 12 mm to ≤ 13 mm on request)	
Straight leads	BRA	CRA
Preformed leads outside crimp	TAR	TCR
Inline wire	YBR	YCR

REEL PACKAGING COMPONENT PITCH 25.4 mm				
		TAPING F		
Lead spacing F		7.5 mm	10 mm	12.5 mm
Body diameter D		> 12 mm	All diameters	
Straight leads	H = 16.5 mm	CRT	DRT	ERT
	H = 18.0 mm	CRU	DRU	ERU
	H = 20.0 mm	CRY	DRY	ERY
Preformed leads outside crimp	H_0 = 16.0 mm	-	TDR	TER
Inline wire	H_0 = 16.0 mm	YRC	YRD	YRE

Note

- The lead diameter of the taped components is depending on the capacitance value and corresponds with the data given in the individual datasheets

AMMO PACKAGING COMPONENT PITCH 12.7 mm		
	TAPING T	
Lead diameter 0.6 mm	H = 18.0 mm straight leads only H_0 = 16.0 mm preformed leads only	
Lead spacing F	5 mm	7.5 mm
Disc diameter D	Valid for ≤ 12 mm standard (> 12 mm to ≤ 13 mm on request)	
Straight leads	BLA	CLA
Inline wire	YAL	YLC

Note

- If a defined product stop is required for mounting on a PCB, a mechanically formed product stop (kinked or inline wire) or a mounting tool should be used